INFLUENCE OF PCB PARAMETERS ON CHIP SCALE PACKAGE ASSEMBLY AND RELIABILITY (PART II)

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ABSTRACT

Current standard surface mount devices such as peripheral leaded packages and area array (Ball Grid Array) devices offer robust assembly yields and good long term solder joint reliability. While standard packages are robust, the drive towards miniaturization continues to force the creation of smaller silicon packaging. When developing a new device or packaging method, it is critical that these must compare to or perform better than standard devices. Not only should the new device perform well in assembly, they must show acceptable package and solder joint reliability in order to gain acceptance and wide use. In an attempt to achieve the functionality and density of bare die assembly, a series of devices known as Chip Scale Packages (CSP), have been developed by the packaging industry which are very close to the dimensions of the bare silicon. CSPs have emerged as an area array packaging alternative for applications requiring low to medium input / output counts on limited Printed Circuit Board (PCB) real estate. Due to their leadless (in general) configuration, larger ball pitch, and compatibility with existing standard surface mount PCB assembly equipment, CSPs avoid a significant segment of the assembly problems encountered in fine pitch peripheral leaded device assembly. While CSPs have been used extensively in low I/O areas such as memory applications, use of CSPs in more demanding environments and applications has been adopted less readily. The trend towards minimal package design is apparent with the release of numerous wafer scale packages, which are often Si die with one or more redistribution layers. With the creation of minimally packaged die (wafer level redistribution), the robustness of the total system "PCB + Device + Solder" must be fully understood in order to ensure the assembly will fill the desired functional role. This paper describes some of the fundamental issues associated with CSP package reliability. Specifically, assembly process parameters, material selection and board geometry affect the yields and reliability during attachment of CSPs onto organic motherboards. Factors such as presence of voids, stiffness of the board and component, board geometry, thermal –mechanical properties, and attachment pad geometry show dramatic differences in accelerated thermal cycle testing. This paper discusses some of the basic assembly and Printed Circuit Board (PCB) parameters that influence the success of CSP assembly and solder joint robustness. In this research, CSPs have been assembled using conventional surface mount techniques and the long-term solder joint reliability has been assessed using accelerated thermal cycle testing and various mechanical testing methods. This paper expands on issues addressed in "Influence of PCB Parameters on Chip Scale Package Assembly and Reliability (PartI)" [Primavera, A. 1999].[1]

Keywords: *Printed Circuit Boards, Chip Scale Packages, Ball Grid Arrays, and Reliability*

INTRODUCTION

Continual miniaturization of electronic components has caused the interconnection between the printed circuit board (PCB) and the component, namely the solder joint, to become significantly smaller as well. Traditionally, the solder interconnection has provided sufficient compliancy to the assembly to allow for the absorption of both thermal and mechanically induced strains in electronics packages. This reduction in the physical size of the joint places more demands on the mechanical properties of the solder to ensure joint robustness. In addition to the footprint size reduction, there is an emphasis on total space reduction, often in the form of reduced size in the packaging of the silicon die. As surface mount technology (SMT) migrates towards smaller package dimensions, the physical and thermal characteristics of each material used in the packaging becomes more critical. Very large differences between properties within a package for example layer to layer, as well as between the carrier and the die lead to large internal stresses within a package. Once mounted onto a PCB, the solder joint must typically absorb all strains induced by the expansion of the package and PCB in thermal excursions. For traditional SMT devices, such as peripheral leaded devices, the leads as well as the solder joint provide the compliance needed to compensate for the mismatch in coefficient in thermal expansion (CTE) of the package and PCB. However, in leadless devices or area array packages, such as ball grid array (BGA) and chip scale packages (CSP), the joints and the structure (PCB and component) must provide CTE mismatch compliance. Currently there are two approaches being used in CSP packaging to increase solder joint thermal fatigue resistance, namely use of a compliant substrate and or interposer, and secondly, the use of the solder itself. As in the trend of many wafer scale CSPs, the joint must provide the compliance since the redistribution layers on the Si package

die are extremely thin and provide little reduction on package stiffness. Additionally, the smaller the joint becomes, the more critical the joint quality becomes. Physical defects such as poor solderability, excessive intermetallic formation, and voids can negatively impact joint robustness and soldering yields. Voids are cavities and bubbles that form within the solidified solder, and may weaken the joint in mechanical, thermal and electrical properties [2]

Factors that affect the assembly and reliability of CSPs are similar to the parameters that affect BGA assembly and reliability. Since most CSPs are smaller versions of BGA packages, the critical parameters that affect BGA should be the same as for CSPs. Factors that affect area array assembly yields could be classified into several main categories [1] including;

Assembly Materials
PCBs and Components
Process Methods
Resulting Joint Quality
Human Factors.

The "Assembly Materials" category can be further sub-divided into solder paste and flux related parameters such as applied volume, reflow parameters, fluxing and solder paste deposition methods, and handling & storage conditions[3]. The most critical issue of this category is to ensure proper fluxing of the attachment surfaces and creation of proper metallurgical bonds during the reflow operation. Improperly formed joints and incomplete metallurgical bonds are very difficult to detect since the solder may physically touch all surfaces to be joined. However, cold joints, which are mechanically connected, but not alloyed or metallurgically connected, may separate and cause early failures in the field. Figure 1 shows an example of a cold joint. The flattened portion of the solder near the attachment pad interface denotes that enough solder was present to physically touch the pad, however, the solder was not bonded to the pad.

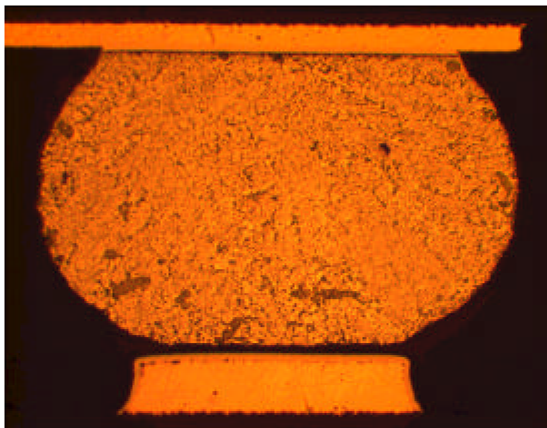

Figure 1 – Cold Joint open following 160 cycles 0-100C 20 minute (5 minute ramp and dwell time) ATC

The "PCB" category contains many influential factors on the overall solder joint reliability including: pad metallurgy, board thickness, pad size, base material, via formation technology, routing method (via in pad versus fan out), PCB layer count, soldermask technology, and pad definition versus mask definition. The "components" sub-group parameters that influences the assembly reliability may include; construction (flex versus rigid carrier etc.), die size to package ratio, solderball size, attachment pad size and definition, base materials, package size, and ball configuration.

The "Process Methods" category is heavily influenced by the individual steps in the assembly. For example, standard double side assembly or a mixed assembly with solder wave pass. Resulting joint quality is a function of almost all assembly variables but is strongly influenced by the type of paste/flux, attachment pad metallurgy and reflow conditions. Highly irregular shaped joints; excessive voiding and poor solderability may lead to early failures. Human factors that are often overlooked may include operator education and training in addition to human error.

1.0 CRITICAL PARAMETERS

One advantage of the CSP package is its compatibility with the existing standard surface mount PCB assembly environment. Typically, current CSP assembly process rely on solder paste deposition through stencil printing, component placement, and mass reflow soldering. In order to ensure high process yields for the assembly process, process parameters that relate to all the above mentioned operations need to be considered. Factors that could affect the assembly process yield can be divided into four main categories including Human Factors, Equipment and tooling, Materials, and Process Methods. These four categories and their sub-categories are described in literature [1], [3], [4], [5], and [6]. Since many of these factors have been presented in literature, only a brief overview of the critical parameters in CSP / BGA assembly is given in the following section.

1.1 Human Factors

Input from operators (including human error) is one of the contributors that can affect the yield of the assembly process. Factors that impact this category include handling, training, education, setup and quality control.

1.1.1 Handling

Improper handling (manual and/or automated) can be detrimental to the integrity of components on the assembly. This issue becomes extremely important when automatic assembly transportation systems (conveyor) are not implemented. Improper manual handling (especially after the component placement process) may result in component misalignment. Consequently, defects such as opens or bridges can occur after reflow soldering. When handling moisture sensitive packages, adequate handling strategies should be implemented to prevent devices from excessive

moisture absorption or damage to circuitry. Popcorning of the device can commonly be attributed to the rapid expansion of entrapped moisture during exposure to high temperatures. Ideally, the device should survive several reflow cycles after being exposed to factory floor conditions during normal scheduled assembly production. Moisture sensitive components may require a pre-assembly bake out in addition to storage in a dry nitrogen chamber. In general, CSPs show almost complete moisture desorption following a 4 – 6 hour bake out at 125C. However, larger devices and moisture sensitive BGAs require bake out at typically 125C for as much as 24 hours.

1.1.2 Setup & Quality Control

A machine's setup does impact the consistency and accuracy of the results obtained. Gage studies should be performed to maintain consistency from line to line and operator to operator. Simple procedures can be implemented to assess the performance of the equipment and operators, these include stencil printing onto a bare laminate before each shift, placing test components onto double sided taped boards, and using a data logger with a thermocoupled board in the reflow oven on a regular basis. More advanced methods could implement assembly of test boards, in process measurement of process variables, and characterization of the placement machine with precision chrome / glass components and boards [7].

1.1.3 Training & Education

Human error can be minimized by a combination of training, proper equipment and tools, and attitude. Operators training not only should focus on equipment, but needs to be extended to include assembly process, and general surface mount issues. Familiarity with the overall process can often help the operators associate with what happens down line from their operation. Mistakes and improper education can affect subsequent operations, and the operators must be able to understand the result.

1.2 Methods

A typical assembly process for area array devices includes: solder or flux deposition, component placement, reflow soldering, and transportation. The methods used for each individual operation are described in detail in [1], [2], [3], [4], [6], [8], [9], and 10]. An introductory description of each is given below.

1.2.1 Solder Deposition

Both paste deposition and pre-formed solder spheres are used to create a solder interconnection between the package and the PCB. While many CSPs utilize a eutectic or near eutectic Sn/Pb solder alloy, a few may utilize a high melting (above 300C) solder alloy balls or columns to prevent the device from collapsing during solder reflow. The eutectic BGA device spheres melt during a standard reflow process and collapse to an equilibrium state. Equilibrium is achieved with the balance between package weight and the buoyant force of molten solder surface tension and wetting forces of the solder with respect to each exposed metal surface. With eutectic CSPs, there is a sufficient amount of solder in the component ball to provide interconnection, however, coplanarity of the device becomes critical to ensure that each bump forms a proper joint. In high melt alloys, any planarity issues associated with the solder ball remain during the assembly since no solder collapse occurs. Therefore, the solder deposition process becomes much more critical to ensure a properly formed joint. In addition, multiple reflows and localized heating from rework operations can cause interdiffusion of the eutectic solder and high lead ball. This can lead to a mixed phase structure and a joint with a gradient of physical and thermal characteristics. Figure 2 shows and example of a high lead solder ball interdiffused with the eutectic paste after 3 rework operations.

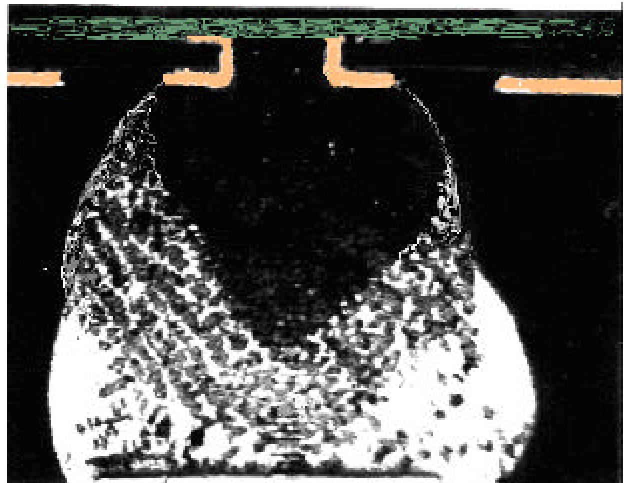

Figure 2 – High melting solder ball interdiffusion.

The most common method for solder deposition in CSP/BGA assembly is solder paste stencil printing. In this process, solder paste is deposited onto the attachment pads of the board through corresponding holes made in a metal foil. For fine pitch CSPs, the printing process becomes critical since there is insufficient room to elongate the solder stencil apertures. Printing circular features greatly reduces the amount of paste transferred through the aperture. For fine pitch CSPs, it is not uncommon to achieve a print efficiency of less than 50 - 60%. Figure 3 shows measured paste deposit volume transfer efficiency (Measured volume / nominal volume) for several 0.5mm pitch and 0.8 mm pitch CSPs, as well as 2 standard 1.27 mm pitch BGAs. The measured data was acquired using an SVS laser inspection system for a 5 mil thick stencil foil. Shown in the graph is the average transfer efficiency for both the CSP and BGA devices. It shows that on average the CSP device apertures transfer 40-60% of the paste (aperture volume). The BGA devices on the other hand show as much as 100% of the nominal paste volume was transferred during the print process. The data is shown for 3 solder pastes. There is a large dependency on paste type as shown in the data. The first 2 pastes were commercially available no clean materials, while the third paste was a water soluble material.

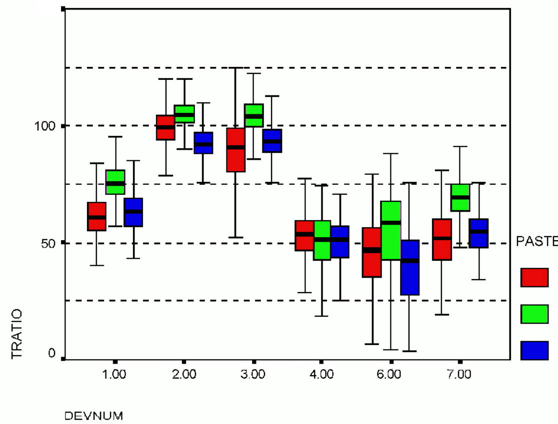

Figure 3 – Typical solder paste transfer efficiency for CSPs and BGAs

1.2.2 Fluxing

Since it is possible to attach collapsible (eutectic) CSP/BGAs without solder paste; attachment methods may additionally include flux deposition. Fluxing for CSPs can be achieved by dipping the component into a flux film deposit, dispensing, spraying, and brush methods. In order to minimize the flux residue left on the PCB following reflow, methods that deposit flux only in the needed areas should be considered. Dipping is commonly used to flux the component balls. In this method, the device ball planarity must be considered when specifying the dip depth. The dip depth must be at least 1 mil (0.0254mm) larger than the ball coplanarity to ensure each bump is fluxed. The flux cleans oxides from the surfaces during the reflow operation.

When a flux only method is used for CSP assembly or rework operations, it is critical to ensure that both the bump coplanarity and warpage of the assembly at reflow temperature is fully understood. The combination of variation in solder ball volume and warpage of both the package and substrate may lead to solder joint opens. If a package has a "small" ball and the device has significant warpage during the reflow, there may not be sufficient solder volume to form a proper joint during the bump collapse. Figure 1, shows an assembly with an open joint due to a combination of package warpage, insufficient solder ball volume, and flux application. The device is a commercially available 144 I/O flexible carrier wirebond CSP with a 0.8 mm pitch. In many cases, the addition of solder paste will help minimize the "small ball" open since the reflown paste can help bridge the gap between the component bump and the PCB attachment pad. While warpage of the PCB is typically small compared to the component substrate, thin boards (0.016") and localized heating can cause significant PCB sagging and or warping. Figure 4 shows the measured component ball side substrate warpage for the package shown in Figure 1. A laser profilometer (Robotics Vision System) was used to scan the package substrate. The average package warpage shown for this device is approximately 2 mils. Several techniques were used to compare the out of plane displacement (warpage). Warpage measurement techniques are discussed and detailed in [11]. In contrast to the component warpage, Figure 5 shows a thin PCB after 2 reflow conditions. The board is FR4 (tetrafunctional), 0.016" thick, 4.5" x 10" and 6 layers in construction with 1 build up layer per side. A 412 I/O BGA was assembled to the topside of the PCB. The post reflow out of plane displacement (measured over a 1.2" component area) was over 10 mils. The PCB was assembled and reflown by use of an edge conveyor only. Use of a PCB pallet limited the sagging/warping to less than 3 mils over the same area.

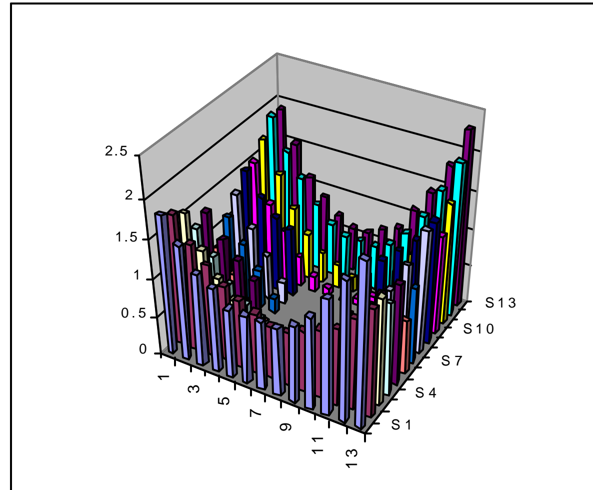

Figure4 - CSP Device Substrate Warpage Measurement

PCB Warpage - Post Assembly

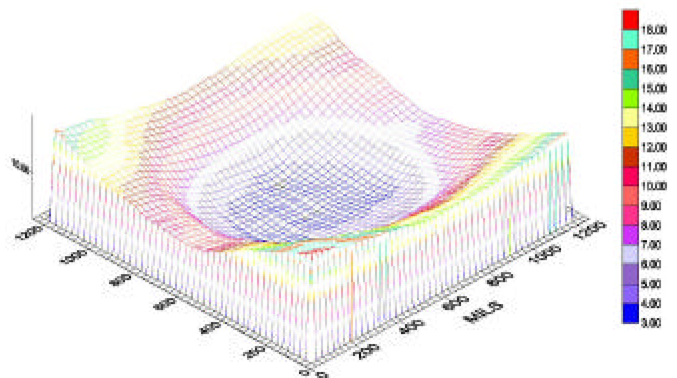

Figure 5 – PCB Substrate Warpage Measurement

1.2.3 Reflow Soldering

Uniformity of temperature across the PCB and within a component is a primary goal of any reflow system. For area array devices, a temperature gradient of 10C or less should be maintained to prevent warpage of the package and to ensure all joints reflow properly. For small CSPs it was

found that infrared reflow system are sufficient to maintain less than a 10C gradient. However IR reflow of BGAs have much larger temperature gradients across the PCB and package due to color differences, surface emmisivity of the devices, and shadow effects. By contrast, forced convection reflow provides a substantially lower temperature gradient across the PCB and BGA solder joint array than infra- red furnaces. Additional issues related to the reflow of BGAs and how it affects assembly yields, see [3], [4], [6] or [9].

1.2.4 Placement

Typically, CSP assembly utilizes sequential component placement. Two types of placement equipment are used for sequential pick and place operations, the first is an X,Y gantry style, and the second is fixed head moving table placement machines. The overhead equipment offers high flexibility, medium placement speed, high accuracy, and minimal accelerations or movement of the PCB. In contrast, the table movement machines (usually rotary turret heads) offer very high placement speeds, medium accuracy, medium flexibility, and impose high accelerations on the PCB. Another important feature of the placement equipment that affects CSP assembly is the equipment vision system. A major issue is the ability of the equipment to recognize features on the board and component and accurately place the device by aligning the device bumps to the attachment pads on the PCB. Another important aspect of the vision system relates to the mis-identification of device features. Some CSPs have logos, nomenclature or other features on the array side of the device. These features may be mis-interpreted as a ball location by a standard forward illuminating camera. Illumination of the package from a lower angle, namely side lighting, may be required to prevent erroneous ball finds on CSPs with bottom side non-ball features.

2.3 Materials

The materials used in the surface mount area array assembly process include solder paste, stencils, components, flux, and the PCB.

2.3.1 Solder Paste

The wet solder paste, after being deposited on the pads on the board, holds the components in place prior to the formation of the solder joint (by reflow soldering). The solder paste, at this stage, temporarily acts as an adhesive. Characteristics of the solder paste that are important from a process perspective including; the solder powder particle size, metallurgy, slump, temperature and humidity sensitivity, solids content, type of flux residue, viscosity, and the propensity for solder balling.

2.3.2 Fluxes

Since the application of flux may be appropriate for CSP assembly or rework, important flux characteristics including viscosity, flux residue, and solids content should be investigated. Screening tests need to be performed to identify potential flux candidates and only those that meet process requirements should be selected.

3.0 Components

CSPs serve the fundamental purposes of any IC package. They provide a metallurgical interconnection between aluminum die bond pads and the solderable metallurgy of a PCB. Simultaneously, CSPs deliver a geometric rearrangement of the IC's bond pads, often resulting in a more relaxed I/O pitch compared to the die bond pads. A CSP is defined as the following:

1. A package that occupies no more than 1.5 times the area (footprint) of the die
2. The individual side geometry is no more than 1.2 times that of the corresponding chip side dimension
3. Package that is direct surface mountable as opposed to the use of wire bonding.

Typically, CSPs provide electrical connections to the PCB in array patterns, on pitches less than 1.0 mm. By design, the package is only slightly larger than the silicon die, thus creating a large thermal expansion mismatch between the device and the PCB laminate. From a reliability standpoint, there are only two types of CSPs, mechanically and non-mechanically decoupled devices. Many of the devices utilize an interconnecting ball pattern that is referred to as a Chip Scale Grid Array (CSGA) [10]. However, from a generic classification of CSPs, they are typically classified into the following five categories:

A. Interposers with a flex circuit interconnect.
B. Interposers with rigid substrates.
C. Lead on Chip (LOC).
D. Wafer-level assembly packages.
E. Wafer-level processes with redistribution.

3.1 Flexible Carrier Devices (Elastomer Interposer)

This style package incorporates a flexible circuit rerouting technique to connect the die bond pads to the solder bumps of the CSGA [10]. The overlay is adhered to the die face with the back of the die exposed. Examples of this CSP type are the Tessera "Micro-BGA" [12], the Chip on Flex package by General Electric, FlexCSP by Amkor, MicroStar by Texas Instruments, as well as a center pad memory module CSP by Texas Instruments [13].

3.2 Flexible Carrier Devices (No Interposer)

A subset of the flexible interposer type CSPs is a die mounted to a polymer substrate without an interposer. Various types of methods are used in the construction of these types of CSPs but most utilize a polyimide flexible, metallized substrate onto which the die is attached using standard die bond epoxy. Packages of this type include; General Electric's Chip-on Flex, Texas Instruments wirebonded Microstar and Memory flex, PacTech's fibre push on flex and Amkor's Flex BGA to name a few.

3.3 Rigid Carrier Devices

Many CSPs are utilizing rigid substrates as interposers in an attempt to push ball grid array component technology into fine pitch / small foot print applications. These devices are typically wirebond dies mounted to a rigid ceramic or organic BGA type interposer. Several flip chip die versions are being developed as well [14]. Several manufacturers are pursuing development of these devices including Matsushita's "Land Grid Array" (LGA), Motorola's "SLICC" (or slightly larger integrated circuit carrier), and Amkor Anam's "Chip Array".

3.4 Lead Frame / Molded Devices

Lead on chip (LOC) technology uses mold resin and support lead frames as package constructing materials which makes the CSP retain the advantages of conventional packages while reducing the size. The technology was developed to decrease the ratios of package to die area and to facilitate the mounting of large memory devices. The other advantage is that it can use dies that are center wire bonded [13] , [15]. Hitachi Cables "Micro Stud BGA", Amkors - ChipSOP and Texas Instruments - Lead On Chip CSP packages are examples of LOC devices.

3.5 Wafer level Assembly Process

Various types of CSPs are manufactured in a wafer format. An example of this type of CSP is Intarsia's Micro-SMT package and Shell Case's - Shell CSP, where the packaging process starts with a finished wafer. In these devices, the majority if not all of the packaging is done on the wafer level and finished devices are diced and shipped.

3.6 Wafer Level Redistribution Process

CSPs that are manufactured using a wafer level assembly process with redistribution layers have solder bumps that are internally connected to the die surface either by columns or by a polyimide circuit redistribution routing layer [10]. Examples of this type of package includes Flip Chip Technologies "Ultra CSP", and National Semiconductors "Micro SMD".

Many component related parameters affect both assembly yields and reliability. Foremost is component construction. The overall material layering and resulting coefficient of thermal expansion (CTE) drastically change the solder joint reliability. In general, solder joint reliability scales with CTE. However, this is not true for elastomer based devices, since the die is physically decoupled from the solder balls. In general, as the packaging of the die decreases, the device CTE becomes approximately that of silicon (namely 2.5 PPM/C). Wafer level CSPs have composite CTE values ranging from 3ppm/C to 5ppm/C, while laminate based CSPs have a ball side CTE of approximately 10ppm/C to 15 PPM/C. An example of the dramatic difference in resulting reliability is shown in [1]. An experiment was performed to study the component construction versus reliability utilizing several packages constructed in the same outline, die size, and bump pattern. The CSP is a 144 I/O 0.8 mm pitch device 12 mm square. The CSP was fabricated using 3 flex carriers, 1 ceramic carrier and 2 laminate carriers. Keeping as many of the remaining parameters constant, ex. Mother board, pad size, pad finish, ball size etc., the laminate packages were shown to last up to 10x longer than the flex device and 100x longer than the ceramic device during a 20 minute 0-100C ATC test. Table 1 shows a comparison of package reliability.

Device	Sample size	0-100C N50	Beta
Flex 1	58	405	6.5
Flex 2	12	434	4.4
Flex 3	35	5300	7.9
Laminate 1	6	2480	6
Laminate 2	24	6300	8.1
Laminate 3	8	5498	7
Ceramic	30	150	2

Table 1 - 0-100C ATC results for Several Packages

4.0 Printed Circuit Board

As shown in [1], [3], [4], and [6], board related parameters influence the assembly yield. Variations in their dimensional parameters can come from various sources including: fiducial deviation, warpage, mask registration, pad size, and pad location deviation (radial deviation). Other factors affecting assembly include attachment pad metallurgy.

4.1 Pad Metallurgy

To prevent pads from oxidation, a solderable layer or coating is deposited on the pad surface. The commonly used pad coating materials include eutectic solder deposited through the Hot-Air-Solder-Leveling (HASL) process, Organic Solderability Preservative (OSP), nickel/gold, nickel / palladium, silver, and tin. These coatings, resulting in different pad finishes, may change the solderability of the pad and, consequently, affect the solder joint's quality. For properly formed joints, a metallurgical bond forms between the solder (Sn) and pad surface (Cu or Ni). During reflow, the Sn combines with Cu or Ni to form an intermetallic layer. While brittle, the layer is extremely strong. For properly formed metallurgical bonds between Cu or Ni and Sn, the interfacial strength is sufficiently higher than the plastic flow stress of the solder. In this case, the solder will rupture or fatigue during thermally induces strains. However, many problems exist that prevent the proper metallurgical reactions to occur. These may include improper amounts of co-deposition materials in the plating baths, oxidation of the underlying pad surface, porosity in the outermost cover layer, organic contamination, soldermask residue, or improper fluxing. This problem will often lead to poor adhesion of the solder ball to the attachment pad. This can result in a very low ball attachment yield, missing solder bumps, time zero joint failures (including dewetting) or weak interfacial strength. In the case of weak interfacial strength, the plastic flow stress of the solder is higher than the interfacial strength and small thermally or mechanically induced strains will cause the solder ball to detach from the pad surface as shown in Figure 6.

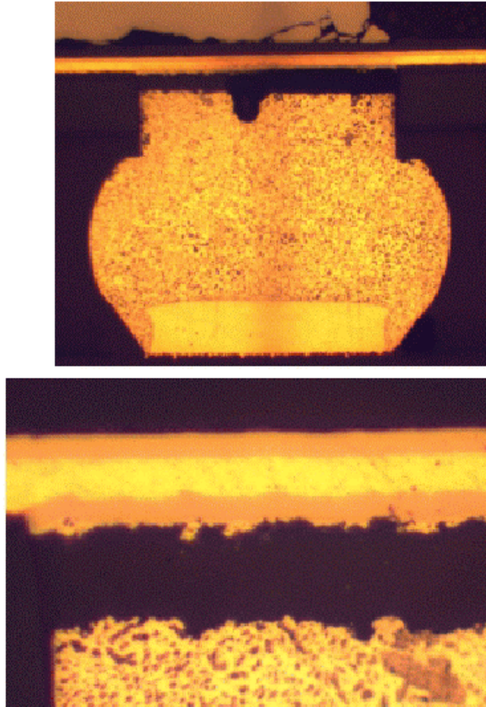

Figure 6 - Time Zero CSP Component Side Failure

A complete load-displacement shear curve should be obtained by a ball shear test in order to evaluate the ball / pad interface [16], and [17]. The ball shear strength required to remove a solder ball with a marginal solder attachment may have an equally high peak shear strength when compared to a "good" joint. It is very important to realize that the "time zero" solder failure is not caused by the same mechanism as joints that embrittle with exposure to elevated temperature. In the later case, the joint degrades well after assembly and only after exposure to elevated temperatures (>100C). Many theories have emerged as to the origins of the high temperature degradation [16], [17], [18], [19], [20] and [21]. It is critical to determine the source of the failure, because poor pad coating can result in solderability problems. Several experiments were performed to evaluate the effect of pad metallurgy on solder joint reliability. A 144 I/O 0.8 mm pitch CSP (wirebond on flex carrier) was used to compare several commercially available pad finishes. The attachment utilized a tacky flux applied by dipping. The PCB was FR4 (135Tg) , 4 layers and 4.5" x 9.5" x 0.062" in dimensions. Attachment pads were 0.3 mm in diameter and pad defined in geometry. The pad finishes considered were: OSP (Entek Plus by Enthone OMI), HASL (Cemco), Pd (immersion) over Ni (electroless), Au (immersion over Ni (electroless), and electrolytic Au/Ni (full body). The ATC was 0-100C and 20 minutes per cycle. Table 2 shows the results from the measured data estimated by a 2 parameter Weibull distribution. As shown, no significant difference in fatigue lives were found.

Device	Metallurgy	Eta (N63)	Beta
CSP144	OSP	460	8.0
CSP144	HASL	470	5.3
CSP144	Au/Ni (immersion)	460	5.1
CSP144	Au/Ni (electrolytic)	390	5.3
CSP144	Pd/Ni	540	9.0

Table 2 – Comparison of Pad Metallurgy

The failures for the CSP144 device are typical fatigue failures although a slight phase coarsening is found in the highly worked crack region (Figure 7). This is not surprising since this device has a very low CTE (5.0ppm/C) and therefore, a high strain load at the solder to pad interface.

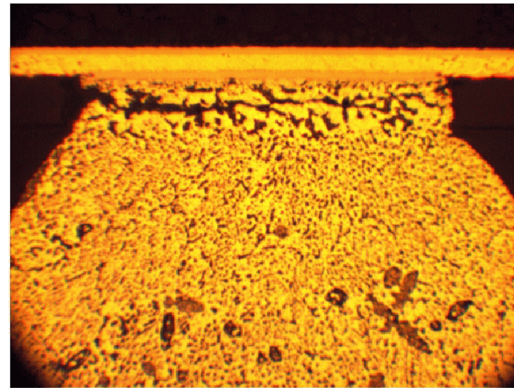

Figure 7 Phase Coarsening Fatigue Failure

4.2 PCB Thickness

A drastic increase in CSP solder joint fatigue lives can be realized by use of a "thin" PCB. When comparing the reliability of CSPs assembled onto 0.062" (1.575 mm) PCBs versus assemblies on 0.016" (0.4mm) or 0.031" (0.8mm thick PCBs, there is a 20% to a 2x difference in fatigue lives [1]. An example of this dramatic difference in reliability is shown in Table 3. The data is shown for a 40 I/O 0.8 mm pitch flex and elastomer carrier CSP assembled onto tetrafunctional FR4 PCBs. The data was generated using a 0-100C ATC test with 5 minute ramp and 5 minute dwell times. Event detection, electrical mapping, dye penetration and cross sectioning methods were used to identify failures. The assembly process for the devices included: solder paste printing using a 5.0 mil (0.127mm) thick stencil, placement by an overhead gantry pick and place machine, and reflow in a nitrogen (less than 50 PPM O_2) convection reflow oven.

Device	Thickness	Metallurgy	Pad Diameter	N63
CSP40	0.031"	Au/Ni	0.014"	3320
CSP40	0.062"	OSP	0.014"	1600

Table 3 – Comparison of 0.031" and 0.062" PCB Thickness on CSP Reliability

4.3 PCB Pad Size

Another equally important PCB parameter that can influence assembly and reliability is the attachment pad size. There is a direct trade-off between yields and reliability when changing pad size. Large attachment pads lead to larger ball collapse and thus can accommodate a much larger ball coplanarity and package warpage. In addition, the placement, self centering of the device, and stencil printing is more robust for large pads. However, that larger pad reduces the effective standoff height for the solder joints. The shear strain imposed on a solder joint is related to the shear angle that the joint is forced to undergo during thermal excursions. A mismatch in the device and motherboard CTE cause thermally induced strains in the solder joints. A reduction in the attachment pad size from 15 mils (0.35 mm) to 12 mils (0.3 mm) shows approximately a 15% improvement in solder joint fatigue life of a flex based 0.8 mm pitch 144 I/O CSP. Table 4, shows the comparison of data. The failure data is for devices assembled onto a 0.062" (1.58mm) thick PCB with Cu OSP pads. The testing was performed in a -40-125C ATC. The cycle was 60 minute with 15 minute ramp and dwell times. Event detection was used to monitor first failure.

Device	Pad	N63
CSP144-2	0.012”	4050
CSP144-2	0.015”	3500
CSP180	0.012”	1227
CSP180	0.016”	906

Table 4 – Pad Size Effect

Another example of pad size effect on package reliability is given in [1], The author shows a 25% increase in fatigue life for a 180 I/O 0.8 mm pitch flex CSP when the attachment pads were reduced from 0.016” to 0.012”. The comparison of fatigue lives is shown in Table 4. It is however possible to make the pads small enough to reduce the joint robustness. In the case of a very small pad, the failure location will shift from the component side towards the board side due to a greatly reduced solder joint area.

Another pad design issue is the use of a via in pad structure. Assembly onto a microvia is becoming a popular alternative to fine line routing. One of the advantages of via in pad technology is the reduction or elimination of traces routed between attachment pads. This allows for a more relaxed soldermask tolerance, reduction of the possibility of exposed conductors, and larger assembly pads. However, one drawback is the fact that voids often form within the solder joint over the via structure. In an extreme case, the void may reduce the mechanical robustness of the assembly. Filling the via with solder before assembly, or plated and filled vias may eliminate this issue.

5.0 Machines and Tooling

The standard surface mount PCB assembly process sequence is sufficient for the assembly of CSP/BGAs. This sequence includes solder paste deposition, component placement, and reflow soldering. Therefore, the equipment considered in this research includes the stencil printer, the component placement machine, and the reflow oven. Also, tooling was designed and made to help achieve the desired process parameters and to facilitate the assembly process. The machines and tooling used, and their effects on assembly yield are described in [1], [3], [4], and [6].

6.0 RELIABILITY RESULTS

While there are dozens if not hundreds of factors that affect CSP assembly yields and solder joint reliability, a few parameters standout as being the most critical. The largest difference in CSP solder joint fatigue was found from the following parameters:

6.1 Board thickness

In general, as the board thickness and overall stiffness decreases, the resulting stress the solder joint experiences decreases. As much as a 2X increase in fatigue life can be realized by assembling CSPs on a “thin board” 0.016” (0.4 mm) versus a thick board 0.062” (1.57 mm).

6.2 Component Device Construction

As the packaging around the die is reduced, the mechanical and thermal properties of the package become more like that of the silicon die. Packages that have a ball side CTE that more closely matches the motherboard PCB, the less thermally induced strains occur.

6.3 Attachment Pad Size

Smaller pads generally give higher reliability while larger pads have a higher yield. Collapse of a eutectic solder ball will be limited by the wettable area of both the device and PCB pads. Ideally, the pads on the package and device should be the same size to allow a uniform joint shape to be formed. A 1-1 pad to device size will give the most spherical joints. The PCB routablity is similarly affected by the pad diameter selection. Smaller pads give more circuit routing space.

6.4 Attachment Pad Metallurgy

For properly formed joints, attachment pad metallurgy shows little difference in solder fatigue lives of CSPs. However, the metallurgical bond must be properly formed on all interfaces. The required intermetallics must be created during the joining process to form a proper bond. In addition, excessive amounts of embrittling agents must not be included such as excessive Au concentrations.

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