

# Optoelectronics Packaging Research at UIC

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## **Abstract**

The present document offers a brief overview of ongoing research into photonic packaging issues within the SMT Laboratory at Universal Instruments Corporation.

The SMT Laboratory is conducting research into issues of particular consequence to the full automation of optoelectronics packaging. The major part of this research is funded by the Area Array Consortium which was established specifically to fund research into design, materials, and process related microelectronics and optoelectronics packaging issues.

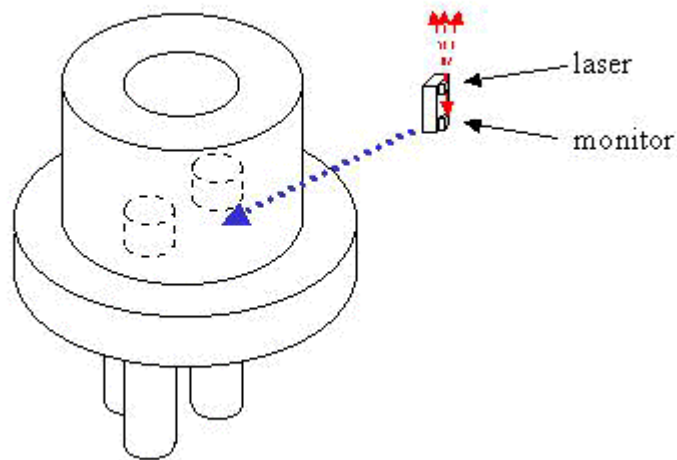
## **Introduction**

The long term aim of our optoelectronics packaging research is to contribute to a transition from the current low volume, partially manual and robot based assembly approaches to a fully automated manufacturing technology of the kind we are used to from microelectronics packaging. This will require a combination of design for manufacturing and quality, materials development and characterization, systems and equipment development, and the development of new types of processes. Obviously, we cannot hope to accomplish all of this by ourselves, but the concurrent developments needed require an understanding of the overall issues by the individual 'experts'. An important component of our work is therefore research to acquire such an understanding, as well as education of our colleagues and students. For the latter purpose we have developed a first 4hour tutorial introducing laser diode packaging concepts from a traditional microelectronics manufacturing perspective. We are currently updating this and complementing it with a tutorial on other (passive) components. In addition, we are working with the local university to develop relevant offerings.

Taking a first look at some of the issues we encounter interesting combinations of high precision (active alignment) and manual or semi-manual assembly practices. In many cases these ensure high performance but often questionable reproducibility or yields.

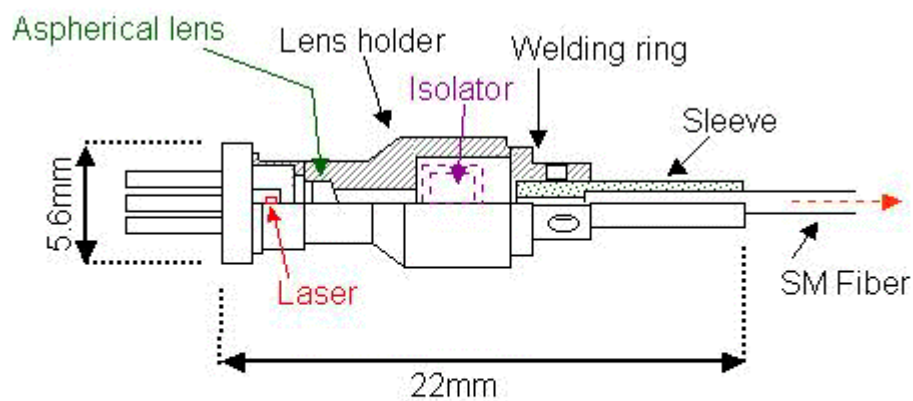
A large number of optoelectronics products would seem to be in great need of better design for manufacturing, at least if one has hope of lowering prices and enlarging volumes through improved automation. Figure 1 shows a sketch of a particularly common, and often not high-end, product: An edge emitting laser and monitor diode attached to a ceramic submount and mounted on a so-called transistor outline (TO) header with the diodes wire bonded to the posts. This is

clearly a question of working with existing parts, rather than designing the most practical configuration. One may argue for the use of one of the few standardized 'platforms' in this industry, but we then commonly have to compensate for the absurdly large tolerances of this product. In the manufacturing of some packages variations in the diameters of the TO headers between 5.3 and 5.6mm did, for example, prevent passive alignment even to multi mode fibers.



**Figure 1. Edge Emitting Laser and Monitor Diode in TO-can**

To underscore the need for design for manufacturing Figure 2 shows an example of a moderately priced package based on a laser in a TO-can. Assembly of this required the active alignment of the laser, lens and isolator to each other and the fiber by simultaneously manipulating the TO-can, the lens holder and the welding ring with the fiber sleeve, then laser welding all these parts to each other. This procedure was obviously quite demanding but still only offered a 50% coupling efficiency!



**Figure 2. 'High Power' Coaxial Laser Module**

## **Research**

So far, our work has included an obvious learning curve involving, among other, teardowns of commercial products and collaborations with photonics manufacturers. We are, however, also researching 1<sup>st</sup>-3<sup>rd</sup> level packaging issues ranging from fiber handling and damage to soldering (AuSn and SnPb) and the deposition, processing, and properties of optical adhesives. Special attention is being paid to the need to pass Telcordia specifications and the consequences thereof.

### ***Teardowns, Product Development and Prototype Assembly***

As an overall reference point, and in order to identify specific relevant research topics, it is important that we continue to work with actual optoelectronics products. This is done in different ways.

We are currently conducting ‘teardown’ analysis of commercial products. This includes both passive and active components: Optical isolators, circulators, laser diode packages, ... Surprisingly often reproducibility and yields are obvious problems and in some cases we can clearly only know the quality of a given part to the extent that that particular one has been tested. In general, potential improvements to current designs and assembly practices come to mind immediately, but so do generic problems, relevant materials characterization projects, etc.

In an extension of this we have also been working with manufacturers to solve individual process and design problems and, in some cases, develop complete products. Finally, we are working towards building generic model components, then assemble these into corresponding ‘prototype products’. This will involve laser attachment to a submount, attachment of submounts to a thermoelectric cooler, fiber alignment and fixing, component assembly, fiber handling and splicing, and so forth. Like the other steps above this is intended to help us formulate future research projects in the same manner as our ongoing consortium work on microelectronics assembly.

### ***Optical Fibers: Splicing, Pigtailling & Connectorization***

A significant 2<sup>nd</sup> and/or 3<sup>rd</sup> level packaging issue is fiber handling and management. Someone has to cleave, strip, clean, pigtail, polish, and usually splice the optical fibers. Any of this, as well as general handling may cause mechanical damage, leading to either immediate fiber breakage or subsequent degradation under unavoidable loads in handling or service. Connectorization may involve alignment through physical contact with a guide groove or conical ferrule, leading to damage and/or maintaining a load on an already damaged fiber. Pigtailling with anything but a quartz ferrule leads to thermal mismatch loads between this and the stripped (damaged) fiber end. Mating of a plug and socket commonly involves compression across the fiber end surfaces, often accompanied by some bending. Attaching a fiber at more than one point along its

length almost certainly couples it with a structure with a different effective CTE than that of silica glass, also inducing stresses.

We are concerned with all of this in two respects. Structures should be designed in a manner to ensure that they can be build without undue damage to the fiber and that unavoidably damaged sections of the fiber are not overloaded in subsequent handling or service. In addition, handling and packaging process 'windows' should be defined to minimize serious damage to the fiber. Economics also makes it important to identify procedures and processes which do **not** cause significant damage, i.e. areas where it is not necessary to 'slow down and be careful'.

We are almost done developing a quantitative understanding of damage and accelerated test approaches allowing predictions of the resulting 'life in service'. Since the minimization or avoidance of damage may often be very costly, such predictions are vital for the proper definition of design and process 'windows'. We have shown the most common current approaches to data interpretation to **overestimate** life in service by several orders of magnitude. Even a few more physically based approaches are seen not to account properly for interactions between mechanical and environmental loads. The consequences for extrapolations of test results depend on the test approach and the anticipated service conditions.

A preliminary version of our approach has been used to assess the damage induced in some typical packaging steps and to suggest corresponding handling, design, and packaging process 'windows'. Stripping was, for example, found to often dominate the mechanical quality (reliability). We are now quantifying the benefits of a new non-contact thermal stripping approach and the meaning of splices passing standard proof tests (see also below). In the long run a major part of our work will, however, address damage in steps such as pigtailling and connectorization, with an emphasis on optimization of processes and designs where needed and proposing general specs.

### ***AuSn Soldering***

Solders used in optoelectronics packaging include PbSn, AuGe, and AuSn, as well as low temperature solders. They all share the obvious advantage over adhesives of not absorbing water and swelling, as well as not densifying with age, thus better maintaining accurate alignments. Soldering of parts included in, or near, the optical path invariably requires a flux less process.

Eutectic AuSn has a lower melting point than the other hard solders but still creeps much less than adhesives and soft solders. The latter is vital for maintaining accurate alignment of structures warped due to CTE mismatches. Another advantage over both adhesives and hard solders is the better thermal conductivity, but this may be sensitive to details of the reflow profile.

Temperature control is extremely important for high performance edge emitting lasers and, since lateral heat conduction within the laser is generally poor, a small void in the solder underneath may easily lead to 'hot spots'. Void free soldering without a flux is, however, by no means a trivial task.

Current AuSn soldering approaches involving active ambients, 'scrubbing', pushing, and holding the assembly within the placement machine during a relatively long reflow process are not really attractive for true high yield, high volume manufacturing. We are investigating the individual requirements and working to reduce or eliminate some of them.

Depending on the application some advantages may be achieved through the use of Au-Sn multilayers, rather than preforms. Notably, the requirements for an active ambient and scrubbing might be relaxed. The use of multilayers will, however, require a careful design of the metallization structures. A thin predeposited AuSn layer (eutectic or slightly Au-poor) offers some of the same advantages without the need to control thicknesses as tightly. At any rate, both thermal conduction and creep properties of the final joint may depend on the reflow profile, as will the practicality of the overall automated assembly process.

The goal of our current efforts is to develop generic recommendations and guidelines for the use of Au-Sn soldering in different types of applications. This requires fundamental studies of the metallurgies associated with different contact pad metallizations, solder structures (single layer solder or multilayers) and reflow profiles. We complement these with measurements of the corresponding materials properties, as well as more applied assembly process development work with preforms, predeposited (near)eutectic layers and multilayers.

### **Adhesives**

Most high volume automated manufacturing of optoelectronics components will almost certainly involve the use of adhesives. This does, however, not come without concerns. Aside from questions relating to hermeticity and outgassing, major issues include dimensional accuracy and stability. The controlled deposition of the extremely small volumes often involved poses a clear challenge. In addition, we find cure kinetics and mechanical properties of cured adhesives to vary with dimensions (bond length and thickness) and assembly configuration in complex fashions. Together, these factors may cause serious assembly-to-assembly variations in the stability of alignment, and they make it much harder and more difficult to extrapolate previous experience and data to new process developments.

A significant amount of work has been done on the fundamentals and realistic performance of the pin transfer process. We are now developing a mechanistic description of the process and its dependencies on materials, design, and process parameters. A similar effort has been initiated on the dispensing of small adhesive dots, the fundamental mechanisms (dynamic wetting) behind which are

essentially the same. In either case we will develop generic guidelines, scalings, etc., for the optimization of the deposition of adhesive dots with diameters on the order of 5mil and/or volumes of 1 nanoliter (1 $\mu$ g) or less. The emphasis of this optimization will be on reproducibility and location control, rather than just on minimizing deposited amounts.

A related adhesive application includes, for example, dipping Au stud bumps on a flip chip VCSEL in adhesive before placing them on corresponding contact pads (see below). The same type of analysis will be applied to this.

We are also continuing our studies of the effect of dimensions and configuration on adhesive cure and resulting properties. The relationship of DSC measurements to the actual cure kinetics are being investigated. Properties of particular concern include creep, moisture uptake and permeability, and optical performance. Effects on, for example, gradual misalignment with time will be studied with model assemblies.

### ***Flip Chip VCSEL***

Future laser diode packaging technology is going to depend strongly on the level of monolithic integration, and on the type of laser (edge emitting or VCSEL) involved. Vertical Cavity Surface Emitting Lasers may not catch up with edge emitting lasers in terms of performance, but they are likely to continue to dominate the large volume markets. They are particularly common in inexpensive products, making the cost of assembly even more of an issue.

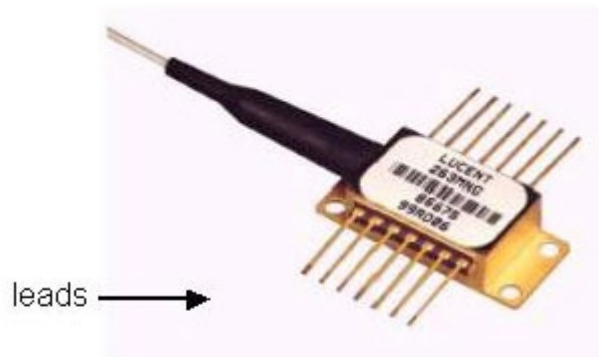
While current products are based on 850nm VCSELs and multimode optical fibers higher wavelength single mode VCSELs are now becoming available as well. This raises the demands on alignment accuracy, but VCSELs are inherently simpler to couple into single mode fibers because of the symmetry of the emitted beam.

A configuration showing considerable promise for both manufacturing and performance, particularly of 1-D and 2-D laser arrays, is flip chip attachment in which bumps on the VCSEL surface are bonded to corresponding contact pads on a printed circuit board or transparent substrate. The VCSELs then shoot into optical fibers on the opposite side of, or embedded within, the substrate. Speeds are enhanced if the electronic driver chip is also a flip chip.

The most common idea is currently to attach the flip chip VCSELs to the substrate through thermo compression bonding of Au bumps, but an attractive alternative from the perspective of volume manufacturing would seem to be soldering or adhesive attach of the Au bumps. We are investigating the issues involved.

### **Selective Soldering**

Butterfly packages (Figure 3) and similarly leaded optoelectronics components are usually soldered to the printed circuit board. This is commonly a manual process with rather high defect levels. Adding to this problem is that defects may be difficult to detect until much later in the overall assembly process. Due, among other, to the sensitivity of common fiber jackets to temperature the package body may often not exceed 85°C, eliminating any chance of using mass reflow. Candidate approaches for automation and defect reduction include hot bar soldering, IR, or selective laser soldering.



**Figure 3. 'Butterfly' Package to be Soldered to PCB**

Somewhat independently of the specific heating approach we have initiated a study of the characteristics of the necessary automated solder (paste) deposition process, the component lead coplanarity and placement process (wetting of all leads, smearing of solder paste deposits), the solder reflow process and the resulting intermetallic formation. Component lead surfaces are typically nickel coated with 1.3-1.5µm or more of electroplated gold, leading to serious gold embrittlement and loss of assembly robustness unless the deposited solder volumes are rather high and the Au is distributed across the entire volume. The gold thickness is usually determined by other factors (simultaneous coating of the whole component) and/or the variability of the electroplating process. Several suppliers claim they can offer much thinner, but still non-porous and reproducible, plated gold layers, but that would have to be verified.

### **Qualification, Robustness & Reliability**

In principle, at least, the successful commercialization of any optoelectronics product almost always requires it to pass standard tests specified by Telcordia. This does not mean that Telcordia claims these to be comprehensive, i.e. the actual product reliability may well be limited by damage mechanisms not tested for within Telcordia specs. In addition, it remains highly questionable whether the Telcordia tests always properly accelerate the mechanisms intended. On the other hand, for the foreseeable future most manufacturers will undoubtedly have

to pass the Telcordia specified tests in order to sell their product. Some of these tests are quite time consuming, i.e. they are not suited for an iterative (empirical) design, process development or materials selection effort.

We are addressing all of this in three ways based on the same overall approach. For one thing we characterize the nature and progression of damage and failure during Telcordia specified tests on model structures representative of realistic products. Based on this we try to develop even faster tests allowing us to 'rank' or optimize individual parameters before submitting the proposed final product for the Telcordia tests, with particular emphasis on the most time consuming ones. In this context it is not vital to **always** have perfect correlation, as final qualification will still be based on the Telcordia tests. Finally, we work to identify realistic damage mechanisms, including creep, likely to affect actual 'life in service' of various products and try to ascertain whether these are indeed addressed and properly accelerated by the Telcordia tests.

A substantial fraction of the qualification issues leading to multiple design cycles of current products are associated with the failure of adhesives in shock, vibration, thermal cycling or storage (damp heat). The latter tests, in particular, may take months. We are paying particular attention to these.

A special concern not addressed very well by Telcordia is the anticipated shipment of die attached and wirebonded subassemblies back and forth between different manufacturing sites (often continents), once true volume manufacturers become involved. This certainly will require an assessment of the robustness and packaging requirements.

In all cases special attention is paid to effects of materials and process variability, as well as of design details.

### **Summary**

Universal Instruments' SMT Laboratory is conducting research into selected design, process, and materials issues deemed to be of particular consequence for the full automation of optoelectronics packaging. These issues currently include fiber handling and damage, selective PbSb soldering, AuSn soldering, and the selection, deposition, and processing of optical adhesives.