

Measurement and Prediction of Reliability for Double-Sided Area Array Assemblies

Anthony Primavera, Ph.D.
Mike Meilunas
Universal Instruments Corporation
Binghamton, NY

James M. Pitarresi, Ph.D.
Shiva Kalyan Mandepudi
Satish Parupalli
Binghamton University
State University of New York
Binghamton, NY

Abstract

The increasing demand for smaller and faster products in the electronics industry has encouraged the use of CSPs and BGAs assembled on printed circuit boards (PCBs) in a back-to-back double-sided fashion. A critical issue in double-sided assemblies is the thermal cycling reliability performance of the device-to-board level attachment. In this paper, the effects of components placed on both sides of the test board were studied. The components included CSPs, BGAs, QFPs and chip capacitors. To assess the assembly flexural stiffness, a three-point bending measurement was performed and the stiffness used as a parameter for investigating the effect of assembly stiffness on the thermal cycling reliability. Cycles-to-failure were documented for all assemblies and the data were used to calculate the characteristic life. In addition, moiré interferometry was used to study the displacement distribution in the solder joints at specific locations in the packages. Data from the reliability and moiré measurements were correlated with predictions generated from three-dimensional finite element models of the assemblies. The models incorporated nonlinear and time-temperature dependent solder material properties and they were used to estimate the fatigue life of the solder joints and to obtain an estimate of the overall package reliability using Darveaux's crack propagation method.

Various configurations of double-sided assemblies were studied. These included symmetrically double sided assemblies (i.e., "mirror image" assemblies), 50% overlap assemblies, and assemblies with an area array component on one side, and chip capacitors (of various sizes) on the other side. In general, a 2X to 3X decrease in reliability was observed for mirror image assemblies when compared to single-sided assemblies for both BGAs and CSPs on 62 mil test boards. The reliability of mirror image assemblies when one component was an area array device and the other was a 208 I/O quad flat pack (QFP) was comparable to the reliability of the single-sided area array assemblies alone, that is, the QFP had almost no influence on the double-sided reliability when

used with an area array component. Generally, the finite element models predicted the assembly reliability within the range expected for Darveaux's method. As building test assemblies and running reliability assessments is both expensive and time consuming, the finite element models can provide a cost-effective alternative to investigating the impact of double sided components on the assembly reliability.

Components and Test Configurations

Seven surface mount devices were utilized in this study. They were:

- 64 I/O CSP with 0.8mm bump-to-bump pitch.
- 256 I/O BGA with 1.27mm bump-to-bump pitch
- 208 I/O QFP with 0.5mm bump-to-bump pitch
- 0402 surface mount capacitor
- 0603 surface mount capacitor
- 0805 surface mount capacitor
- 1206 surface mount capacitor

A daisy-chained 0.062" thick printed circuit board (PCB) was used in the assemblies. Solder mask protected traces are located on the top and bottom surfaces of the test board and connect each device to a gold edge finger connector that is utilized to interface to an event detector. Additional traces run from the various points within the daisy chain to exposed probe pads located around the perimeters of the device footprints. These probe pads were included to facilitate testing by isolating the solder joints within the assembly to sets of two or three bumps. The pads were approximately 0.0022" thick. The test boards were supplied with a copper OSP surface finish.

A standard print-place-reflow process was used to assemble the surface mount devices to the PCBs. 63Sn/37Pb paste was stencil printed over the test board pads using a laser cut stainless steel stencil. Components were placed and then reflowed in a ten zone forced convection oven using a nitrogen atmosphere with an oxygen level less than 50 ppm.

Eight basic test configurations were assembled. The CSP family assemblies used a 0.93" x 0.93" PCB coupon while the BGA and QFP assemblies used a 1.73" x 1.73" PCB coupon. The eight main configurations were:

- Single-Sided CSP using 0.012" diameter non-solder masked defined (NSMD) PCB pads.
- Double-Sided "Mirror Image" CSP using 0.012" diameter NSMD PCB pads.
- Double-Sided "50% Offset" CSP using 0.012" diameter NSMD PCB pads (see Figure 1).
- Front-side CSP with 0.012" diameter NSMD PCB pads and back-side capacitors. The back-side capacitor array consisted of 31 devices. Four different capacitor configurations used: 0402, 0603, 0805 and 1206 (see Figure 2). Note that capacitor performance was not monitored during reliability testing.
- Single-Sided BGA assembled using 0.020", 0.022" or 0.024" NSMD pads.
- Double-Sided "Mirror Image" BGA assembled with 0.020" or 0.022" NSMD pads.
- Front-side BGA assembled using 0.022" or 0.024" NSMD pads with backside QFP assembled to 0.012" x 0.060" rectangular NSMD pads.
- Single-Sided QFP assembled with 0.012" x 0.060" rectangular NSMD pads.

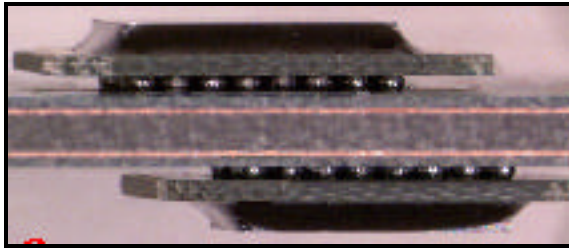


Figure 1
Side view of 50% off-set CSP assembly.

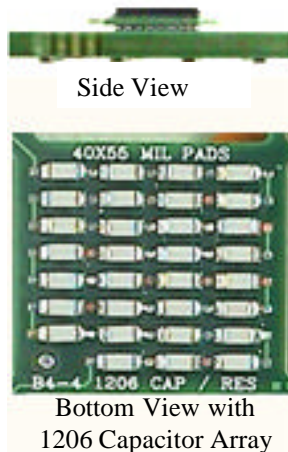


Figure 2

Typical backside chip capacitor array.

Stiffness Measurements

The three-point bend test was used to determine the stiffness of various assemblies studied in the paper. Because stiffness is partly a function of geometry, two baseline conditions were established: one for the 0.93 x 0.93" PCB and one for the 1.73 x 1.73" PCB.

Bend testing was performed using a universal testing machine. A fixture was used to provide edge support along two opposing sides of the PCB assembly, as shown in Figure 3. Assemblies were placed over the edge supports with the populated side (if any) facing down. During testing the loading velocity of the probe was maintained at 0.100" per minute and the force was recorded. From this data, force versus displacement curves were plotted for each assembly and stiffness was calculated as the slope of the force/displacement plot in the linear region.

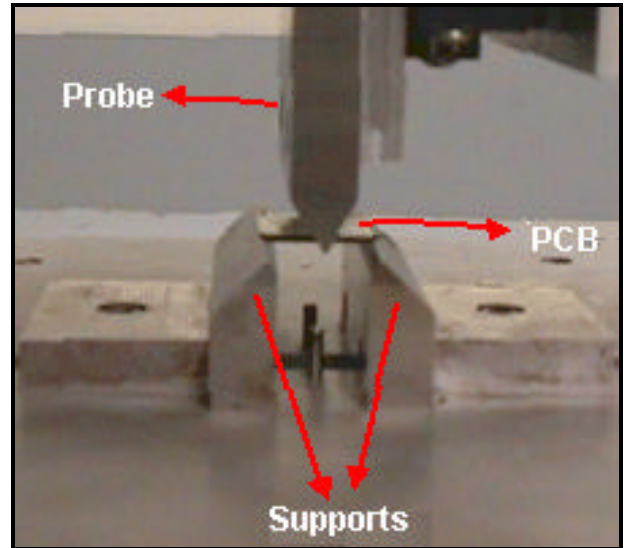


Figure 3
Test fixture for measuring coupon stiffness

Only bare PCBs and single-sided assemblies were evaluated. The 1.73" PCBs were supported at 1.60" spacing while the smaller 0.93" boards were supported at 0.85" spacing. Eight to ten measurements were taken for each assembly type and the average stiffness was calculated. Results are summarized in Table I.

As expected, testing clearly showed that the stiffness of the smaller PCB assemblies was greater than that of the larger PCB assemblies due to geometrical differences and support spacing. This does not indicate that the reliability of a CSP assembled to the smaller PCB is lower than the reliability of a CSP assembled to the larger PCB, but instead stresses the importance of the bend test methodology.

Table I
Average Measured Stiffness of Test Coupons

Assembly Description	Measured Stiffness (lb/in)	
	1.73" x 1.73" Assembly	0.93" x 0.93" Assembly
Bare PCB	1,100	3,250
PCB with 0402	-	3,333
PCB with 0603	-	3,420
PCB with 0805	-	3,447
PCB with 1206	-	3,671
PCB with CSP	-	5,000
PCB with BGA	2,964	-
PCB with QFP	2,375	-

The bend tests showed that the stiffness of the BGA assembly was 2.7X greater than its bare PCB counterpart while the QFP assembly was nearly 2.16X stiffer than the bare board. Bend testing of the 0.93" x 0.93" PCB assemblies showed that the bare PCB assembly had the lowest stiffness while the 0402, 0603, 0805 and 1206 capacitor arrays resulted in successively stiffer assemblies. The PCB with the attached CSP had the highest stiffness of the group, as expected.

Accelerated Thermal Cycle

For this phase of the investigation, a 30-minute, 0°C to 100°C air-to-air thermal cycle (AATC) was utilized. The thermal cycle consisted of 5-minute dwells at the temperature extremes and 10-minute transition periods (+/-10°C/min). Temperature variation within the thermal chamber conformed to the IPC-9701 standard.

The test assemblies were loaded into a thermal cycling chamber and attached to an event detection system (EDS). The EDS continuously monitored the electrical integrity of the test assembly and recorded electrical “events” or momentary resistance changes that surpass 300 ohms for a minimum duration of 200 nanoseconds. Failure was defined per IPC-9701 that requires the first event be confirmed by nine additional events within 10% of the cyclic lifetime.

The following assembly combinations were evaluated by AATC:

- Single-Sided CSP
- Double-Sided “Mirror Image” CSP
- Double-Sided “50% Offset” CSP
- CSP with Backside Capacitors
- Single-Sided BGA
- Double-Sided “Mirror Image” BGA
- BGA with Backside QFP
- Single-Sided QFP

The characteristic life of the assemblies was computed using WinSmith’s Weibull software. In addition to the combinations listed previously, the difference between similar package types subjected to one reflow versus two reflows was considered, but was found to have little impact on the present study.

Table II summarizes the reliability measurements of the assemblies without considering the effect of multiple reflows. From this table it is apparent that:

- The single-sided CSP had the highest reliability among all CSP samples.
- The addition of progressively larger backside capacitors decreased the reliability of the CSP.
- The double-sided “Mirror Image” CSP was the least reliable CSP assembly
- The double-sided “50% Offset” CSP assembly performed 26% better than the “Mirror Image” assembly, but still performed considerably lower than any other CSP assembly.
- Single-sided BGA assemblies were comparable to the BGA/QFP assemblies.
- Double-sided “Mirror Image” BGA assemblies were 3X less reliable than the single sided BGA assemblies.
- Neither the single-sided QFPs nor the QFPs used in BGA/QFP assemblies failed.
- A backside QFP did not adversely affect the reliability of a topside BGA.
- Increasing PCB pad diameter while keeping the solder volume constant resulted in decreased BGA reliability.

Table II
Measured Cycles-to-Failure

Assembly Description	Cycles-to-Failure (N ₆₃) PCB Coupon Dimensions	
	1.73" x 1.73"	0.93" x 0.93"
CSP	-	6,140
CSP with 0402	-	5,837
CSP with 0603	-	5,369
CSP with 0805	-	5,146
CSP with 1206	-	5,069
CSP and 50% Offset CSP	-	3,026
Mirror Image CSP	-	2,396
BGA (0.020" Pad)	8,284	-
BGA (0.022" Pad)	7,897	-
BGA (0.024" Pad)	7,736	-
Mirror Image BGA (0.020" Pad)	2,890	-
Mirror Image BGA (0.022" Pad)	2,719	-
QFP	>10,000	-
BGA (0.022" Pad) with QFP	8,161 (BGA)	-

BGA (0.024" Pad) with QFP	8,010 (BGA)	-
------------------------------	-------------	---

The data accumulated from AATC was correlated with the bend test results to study the effects of assembly stiffness on surface mount reliability of the CSP assemblies. The increase in stiffness (from Table I) of the CSP coupons above that of the bare PCB is tabulated with the decrease from the single-sided CSP assembly reliability (from Table II) with the results are shown in Table III. It is noted that bend testing was not performed on double-sided assemblies. Consequently, the stiffness increase reported in Table III represents the change in stiffness above that of the bare PCB test coupon. For example, the increase in stiffness due to the attachment of a CSP on the coupon is given by: 5,000 lb/in minus 3,250 lb/in giving 1,750 lb/in. Therefore, it is tacitly assumed that a double-sided mirror image CSP would therefore have a bend stiffness of: 3,250 lb/in (bare PCB) plus two CSPs, each increasing the stiffness of the assembly by 1,750 lb/in giving a total assembly stiffness of 6,750 lb/in. This hypothesis will be tested in future work. The data are also plotted in Figure 4.

Table III
CSP Coupon Assembly Stiffness and Reliability Data

Component Added to Assembly	Stiffness Increase (lb/in)	Reliability Decrease from Single-Sided CSP (cycles)
0402 Chip Capacitors	83	303
0603 Chip Capacitors	170	771
0805 Chip Capacitors	197	994
1206 Chip Capacitors	421	1,071
CSP	1,750	3,744

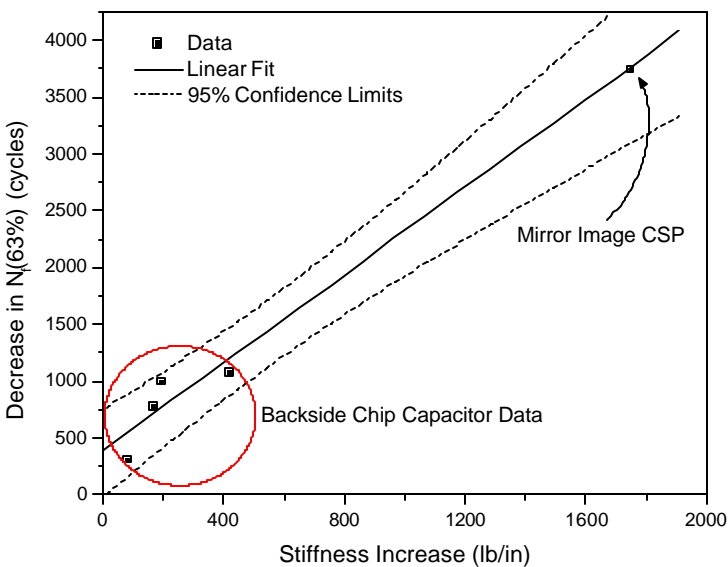


Figure 4

Decrease in Assembly Reliability vs. Increase in Assembly Stiffness for the CSP test coupons.

The regression coefficient for the linear best-fit line is 0.99 and its equation is given as:

$$\Delta N_f = 364 + 1.93\Delta K \quad (1)$$

where ΔN_f is the *decrease* in the CSP assembly cycles-to-failure (cycles) and ΔK is the *increase* in assembly stiffness (lb/in). As a test, the regression analysis was repeated using only the four chip capacitor data points. The predicted change in the reliability was within one percent of that using the entire data set.

A similar trend was observed when comparing the single-sided BGA assembly to the double-sided BGA assembly. Interestingly, the stiffness/reliability relationship did not hold true for BGA/QFP assemblies. Although the bend test indicated that the stiffness of the BGA/QFP assembly was 2.16X stiffer than the single-sided BGA assembly, no negative reliability impact due to the QFP was observed. This is possibly due to bend test methodology and mechanical behavior of the QFP. The bend test measured stiffness in the z-axis (i.e., out-of-plane direction) while the response of the QFP body in AATC is primarily in the in-plane directions. Additionally, any stiffness effect must be transferred to the PCB and then to the BGA through the compliant QFP device gullwing leads. Also, the effect of the QFP may have been further diminished because the entire solder bump array of the BGA was located within the QFP attachment outline as shown in the footprint of the two packages in Figure 5.

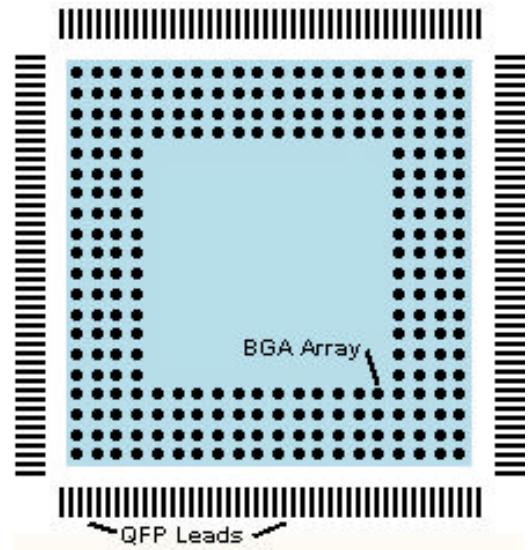


Figure 5
QFP Lead vs BGA solder array location.

Finite Element Modeling

To assist with the understanding of the AATC response and to extend the current modeling approaches to include double sided assemblies, finite element models were constructed of the single-sided and mirror image CSP and BGA assemblies, as well the 50% offset CSP assembly.

Accurate constitutive modeling of the solder plays an important part in the solder joint reliability model. Unifying plasticity and creep via a set of flow and evolutionary equations Anand developed a constitutive model for hot working of metals [1]. There are two basic features in Anand's model applicable to isotropic rate-dependent constitutive model for metals. First, there is no explicit yield surface. Rather, the instantaneous response of the material is dependent on its current state. Secondly, it assumes plasticity from the very beginning of the analysis. The inelastic strain rate in Anand's definition is dependent on temperature and stress.

Anand's model, in its original form, did not consider rate-independent plasticity. Therefore, Darveaux, et al. [2] were the first to modify the constants in Anand's constitutive relation to account for both time-dependent and time-independent phenomenon. Parameters for near-eutectic 62Sn/36Pb/2Ag solder are given in [6, 7].

Anand's constitutive model in ANSYS® requires the use of an element capable of viscoplastic response. Such element types are available for both two- and three-dimensional modeling in ANSYS®. In addition, these elements have, as a standard output, viscoplastic work. This parameter was used in the solder fatigue model employed in this paper.

For the single-sided assembly models, octant symmetry was used. A typical single-sided model, in this case the BGA assembly, is shown below in Figure 6.

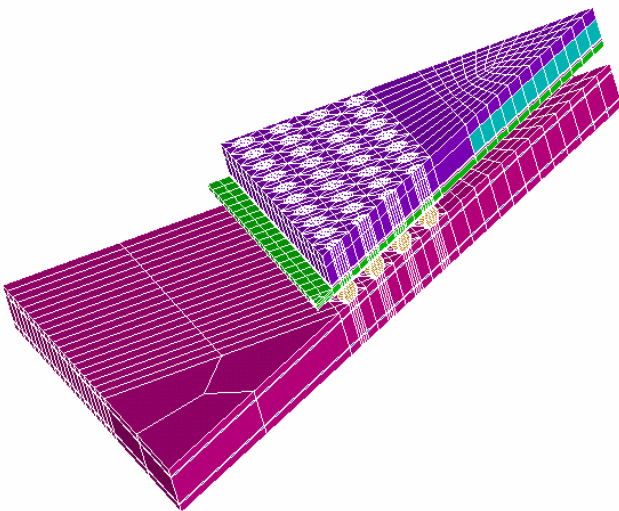


Figure 6

Octant symmetry finite element model of the single-sided BGA assembly.

The 50% offset CSP could not be modeled using octant symmetry. Consequently, Figure 7 shows this model using simple centerline symmetry.

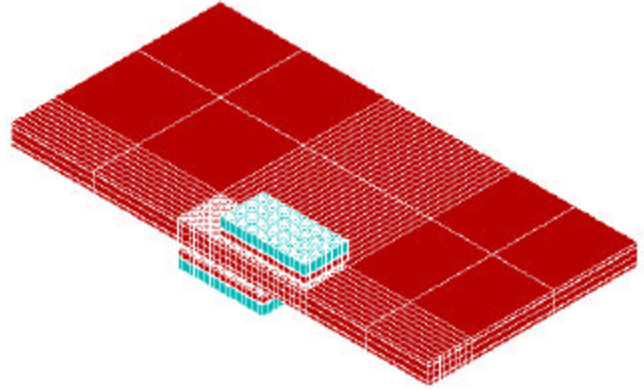


Figure 7
50% offset CSP model.

Moiré Measurements

Moiré interferometry is an optical technique for measuring displacement in a specimen. The results of a moiré analysis are full-field in-plane displacements in the form of a fringe pattern viewed on the surface of the specimen. The equations that govern the relationship between fringe order and in-plane displacement are expressed as:

$$U = \frac{1}{f} N_x$$

$$V = \frac{1}{f} N_y$$

Here U and V are the in-plane displacement fields in the x - and y -directions, respectively, and N_x and N_y are their respective fringe orders. The quantity f is the frequency of the reference grating. For electronic packaging applications the in-plane displacements can be measured with an accuracy of 0.417mm per fringe order. Computer processing of the image data can enhance the resolution of the fringe orders [5].

The assemblies were cross-sectioned to expose a row of solder joints for moiré displacement analysis. The sample and grating (mounted on an ultra-low expansion glass substrate) were pre-heated in an oven at the 100°C . The sample and grating substrate were then removed from the oven and a thin, even layer of high temperature, low viscosity epoxy was applied to the surface of the sample using an optical grade tissue. The sample was then pressed onto the substrate and placed back into the oven to cure the epoxy [5]. Care was

taken to ensure that the sample was not out of the oven for an extended period, as this can lead to errors in the measurement [6]. Once the epoxy was cured, the sample and substrate were taken from the oven and the substrate was removed from the sample, leaving the grating attached to the sample. The sample then cooled to room temperature. A typical assembly from this study was instrumented with a thermal couple and the cool down curve was recorded and is shown in Figure 8.

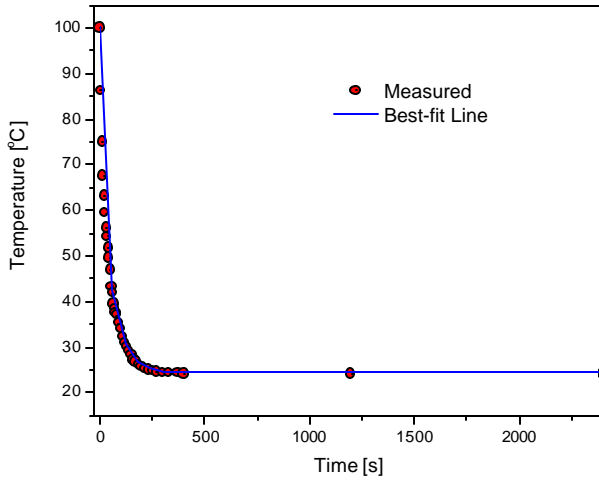


Figure 8

Typical measured cooling curve of an assembly.

Once the part was cooled, it was placed into the interferometer. After setup and calibration, the fringe-shifting technique was used to obtain a series of interference pattern images [5]. These were post-processed to determine the fringe patterns indicating the desired contours of displacement. A typical moiré pattern is shown in Figure 9 for the single-sided BGA assembly. Using the cool down curve from Figure 8, a finite element model of the moiré sample was subjected to the same loading and boundary conditions. The predicted horizontal displacement in the worst case solder joint (die shadow) was $114 \mu\text{in}$ while the measured displacement via moiré was $98.5 \mu\text{in}$. This represents approximately a 15% difference indicating very good correlation.

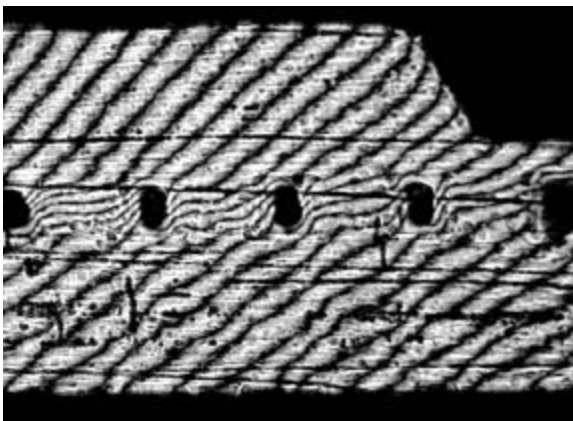


Figure 9

Moiré horizontal displacement fringe pattern of single-sided BGA assembly (right side shown).

The double sided BGA assembly was also modeled and moiré images were obtained (Figure 10). In this case, the predicted displacements were within approximately 25% of the measurement. Again, this good correlation between the model and measurement inspires a certain level of confidence in the models. Consequently, in the next section, the models were used to predict the fatigue life of the single- and double-sided assemblies.

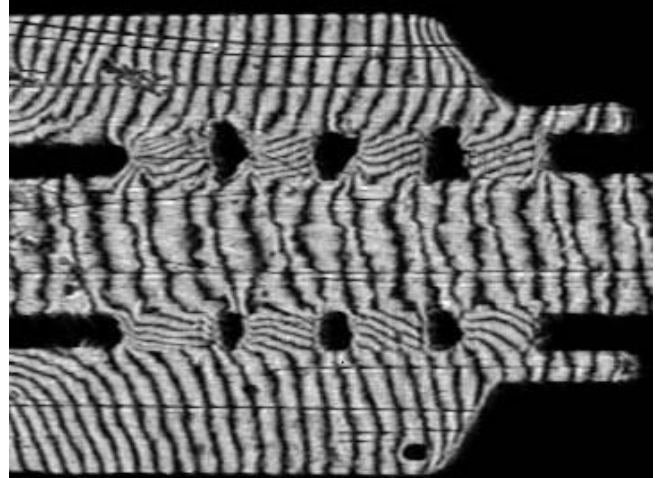


Figure 10

Horizontal displacement moiré fringe pattern of double-sided BGA assembly (right side shown).

Finite Element Reliability Prediction

In addition to solder constitutive modeling an energy-based metric for predicting crack initiation and growth in solder joints was also developed [2]. Over the years, this method has been further refined [3, 4]. The two major constituents of the crack growth rate model are N_o (the number of cycles to crack initiation):

$$N_o = A\Delta W_{ave}^B \quad (2)$$

and da/dN (crack growth rate per cycle, N):

$$\frac{da}{dN} = C\Delta W_{ave}^D \quad (3)$$

where A , B , C , D are constants that dependent on material and element size and ΔW_{ave} is the volume averaged viscoplastic strain energy density increment. The two major constituents are combined to predict the characteristic fatigue life (N_a) of the joint, thus:

$$N_a = N_o + \frac{da}{dN} \quad (4)$$

At the corner of the solder joint and pad for typical ball-type joints, certain stress and strain components (and therefore viscoplastic work) show a high degree of sensitivity to the element size used to model that region. Consequently, convergence studies were performed guidelines for element thicknesses at this critical interface were suggested [3, 4]. From these guidelines, a mesh of elements with acceptable aspect ratios is then constructed. Darveaux's technique accounts for the singularity problem at the interface by a two-pronged method. First, the four constants (*A*, *B*, *C*, *D*) used in Eqns. (2) and (3) were identified for a range of element thickness as shown in Table III. Second, the stabilized viscoplastic strain energy density per cycle was extracted after the third thermal cycle of the simulation and then volume averaged across the crack interface.

Table III

Suggested constants for use in predicting 62Sn36Pb2Ag solder fatigue with Eqns. (2) and (3) [3,4].

Thickness Along Interface [0.001"]	<i>A</i>	<i>B</i>	<i>C</i>	<i>D</i>
0.5	71,000	-1.62	2.76	1.05
1.0	56,300	-1.62	3.34	1.04
1.5	48,300	-1.64	3.80	1.04

The reliability or number of survivors, for a two-parameter Weibull distribution is as

$$R = e^{-\left(\frac{N}{N_a}\right)^b} \quad (5)$$

where *R* is the reliability, and *N* is the number of cycles to achieve that reliability. The two parameters are *N_a* (the characteristic life), and *b* (the shape parameter or Weibull slope). For a series of joints connected electrically, the overall reliability of all the joints is given by the product of the reliability of each joint in the series. With the characteristic of each joint computed from the finite element calculations using the crack growth rate approach, the cycles-to-failure versus reliability relationship can then be generated for any assumed shape parameter. A fixed Weibull slope of 4.0 was assumed in all models.

By simulating the AATC, the finite element models were used to estimate the viscoplastic work per cycle in the solder joints. From this, Darveaux's crack propagation method was used to determine the life of the solder joints. Using the Eq (5), it was then possible to estimate the assembly reliability. Results from the AATC finite element simulations for the single-sided and

mirror image BGA and CSP assemblies, as well as for the 50% offset CSP are presented in Table IV.

Table IV

Summary of assembly *N_f*(63%) reliability predictions.

Assembly	Reliability (cycles)	
	Measured	Predicted
Single-Sided BGA (20 mil pad)	8,284	8,153
Single-Sided BGA (22 mil pad)	7,897	7,991
Single-Sided BGA (24 mil pad)	7,736	7,814
Mirror Image BGA	1,576	2,890
Single-Sided CSP	7,611	6,140
Mirror Image CSP	3,174	2,300
50% Offset CSP	3,026	3,000

As can be seen in Table IV, the predicted reliabilities were in very good agreement with measurements. The finite element models were also successful at capturing the subtle trend of decreasing reliability with increasing pad size, as was observed in the measurements. It is noted that the predicted reliability for the mirror image BGA was very conservative, yet it was still within the ±2X expected range of the measured values. These results indicate that the Darveaux crack propagation methodology can be successfully extended to finite element reliability modeling of double-sided assemblies.

Conclusions

Various configurations of double-sided assemblies were studied in this paper. These included symmetrically double sided assemblies (i.e., "mirror image" assemblies), 50% overlap assemblies, and assemblies with an area array component on one side, and chip capacitors (of various sizes) on the other side. In general, a 2X to 3X decrease in reliability was observed for mirror image assemblies when compared to single-sided assemblies for both BGAs and CSPs on 62 mil test boards. The reliability of mirror image assemblies when one component was an area array device and the other was a 208 I/O quad flat pack (QFP) was comparable to the reliability of the single-sided area array assemblies alone, that is, the QFP had almost no influence on the double-sided reliability when used with an area array component. The finite element models had very good correlation with the predicted assembly reliability and all predictions were within the range expected for Darveaux's method. As building test assemblies and running reliability assessments is both expensive and time consuming, the finite element models can provide a cost-effective alternative to investigating the impact of double sided components on the assembly reliability.

Acknowledgments

The authors (JP, SKM and SP) wish to thank Universal Instruments Corporation for their generous technical and financial support of this research project. The continued support of the Integrated Electronics Engineering Consortium (IEEC) of SUNY/Binghamton is also gratefully acknowledged. ANSYS® is a registered trademark of ANSYS, Inc.

References

1. Anand, L., "Constitutive Equations for Hot-Working of Metals", *International Journal of Plasticity*, Vol 1, pp. 213-231, 1985.
2. Darveaux, R., Banerji, K., Mawer, A., and Dody, G., "Reliability of Plastic Ball Grid Array Assembly", Ball Grid Array Technology, J. Lau, ed., McGraw-Hill, NY, 1995.
3. Darveaux, R., "Solder Joint Fatigue Life Model," Proc. *TMS Annual Meeting*, Orlando, FL, pp. 213-218, 1997.
4. Darveaux, R. "Effect of Simulation Methodology on Solder Joint Crack Growth Correlation," *ECTC*, Las Vegas, NV, pp. 1048-1063, 2000.
5. Post, D., Han, B., Ifju, P., High Sensitivity Moiré, Springer-Verlag, New York, 1994.
6. Rayner, J. and Pitarresi, J.M., "Sample Preparation for Moiré Interferometry," *Soc. Exp. Mech.*, Cincinnati, OH, June, 1999, pp. 11-14.