Flip Chip Research – Who Needs It?

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Introduction

Flip chip technology has yet to reach full maturity and many aspects remain incompletely understood. Even the most experienced practitioners often run the risk of unpleasant surprises or, at the very least, unnecessarily low assembly yields. The only way to address this, as well as hopefully have the resources to 'fight some of the fires', is to maintain a sizable research effort. A couple of the many reasons are illustrated below.

Content

Over the past 7 years an international consortium of top-tier companies (currently 32) have been funding research at Universal Instruments addressing a broad range of issues: Consequences of chip layout, attachment alternatives (solder, adhesives), UBM selection, wafer bumping, backlapping, dicing (defects), flux selection and process, placement, reflow ambient and profile, lid attach, and overmolding. Particularly large efforts emphasize no-Pb issues and substrate technologies, and current topics include new optoelectronics applications.

Unique to flip chip are the small dimensions and the need to underfill. The codification of the underfill process alone currently approaches a hundred pages. Although strongly dependent on it, this does not directly address reliability issues. In the absence of a fundamental understanding these can be extremely confusing or readily misinterpreted. For example, different size chips often exhibit different reliability but this has nothing to do with distance-to-neutral-point, like in most other types of assembly. While still sensitive to the joint properties, flip chip reliability usually depends even more on the underfill. Years of fundamental studies, plus testing and detailed failure analysis of tens of thousands of assemblies, have helped us understand the interdependent effects of materials combinations (flux, underfill, solder mask, solder and pad metallurgy, laminate, chip passivation, ...), design (joint layout and dimensions, mask openings, pad configurations, ...) and process parameters (bakeout, fluxing technique and volume, cure conditions, fillet design, dispense parameters and variabilities, ...). Even when thermal excursions are important reliability is often dominated by aging and humidity effects which are not well accounted for in common accelerated tests. Electrical failure usually involves solder fatigue or bridging, but strongly affected by underfill cracking, solder extrusion into voids or cracks in the underfill, and/or delamination from one of the stress concentration locations in **Figure 1**. To our knowledge no one has yet been able to account for these competing mechanisms in extrapolating accelerated test results to life in service with any degree of credibility. However, we are currently defining appropriate test procedures and expect to make first, conservative, extrapolations relatively soon. The consequences for many potential applications are likely to be tremendous.

In several respects the small dimensions make flip chip assembly particularly sensitive to aspects of design, tolerances, and process variations. Sadly, although the difficulty of repair may make yield assessment and optimization quite critical, flip chip substrate designs are rarely optimized to account for known tolerances. Rather, design and process optimization is often based on experience and/or empirical extrapolations. This has, at times, been dangerously misleading. In general, almost all of the process steps mentioned above may contribute to the overall defect level and our current research efforts include assessments of the contributions of all of them. In the following we report examples of the use of a couple of the tools (computer programs) developed to help assess the combined effects of some of the many statistical parameter variations (tolerances) and to optimize substrate and process design to account for these.

Overly optimistic claims are often made as to the benefits of solder joint self alignment. **Figure 2** shows predicted defect levels for an 8 mil pitch perimeter array chip with eutectic Sn-Pb bumps placed on a conventional PCB with typical tolerances. For an 8 mil (or less) wide solder mask opening the high defect level is dominated by solder mask misregistration and insensitive to placement accuracy. On the other hand for an optimized pad design yields are insensitive to trench widths above 10-11 mil, but a placement accuracy $\sigma_m < 0.25$ mil is preferred. Finer pitch chips require tighter solder mask tolerances, prohibitively large mask openings, or an alternative substrate technology. Even then, unless pad size tolerances are also improved 6 mil pitch chips may require $\sigma_m < 3\mu m$!

Another potential source of defects is bridging or opens due to the combined effects of solder bump height variations, substrate pad thickness and size variations, solder mask opening variations, and substrate warpage in reflow. These effects depend on substrate technology and pad design. At moderate and large pitches designs are readily optimized to ensure low defect levels with achievable (tight) eutectic solder bump height distributions. However, this becomes increasingly challenging for finer pitches, alternative substrate technologies, most no-Pb solders, and/or attempts at cost savings through, for example, reflow in air.

Consider, for the sake of illustration, the selection of substrate supplier and design for the 6 mil pitch chip in **Figure 3**. The best achievable solder bump height distribution here had a mean of 3.5 mil and a standard deviation of 3%. The available (and affordable) substrate technologies allowed for two different via-in-pad designs: A mask-defined design with smaller solder mask openings over 5 mil diameter pads, and a pad-defined design with smaller pads/traces through larger solder mask openings. Assuming a quoted standard deviation of 0.25 mil in pad and solder mask opening size and a substrate warpage of 0.3 mil across the die region, the two designs were optimized to minimize defects. At this point the mask-defined design was predicted to lead to about 20 ppm opens.

Experience shows, however, that many high density substrates tend to warp more than that. A warpage of 0.5 mil would lead to 0.1% defects for the mask-defined, but only 1 ppm for the pad-defined design. Returning to the question of placement related defects even a placement machine with $\sigma_m < 3\mu m$ was found to require sloping walls of the solder mask openings to prevent the solder bumps from getting ‘stuck’ too often, suggesting a supplier using laser ablation to make the openings.

Conclusion

Who needs it? Most practitioners eventually.

Figure Captions

Figure 1: Flip chip with origins of competing underfill damage mechanisms.
Figure 2: Placement related defects vs. placement accuracy for two mask openings.
Figure 3: 11mm flip chip with 6 mil pitch within and between rows.

Company

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Figure 1.

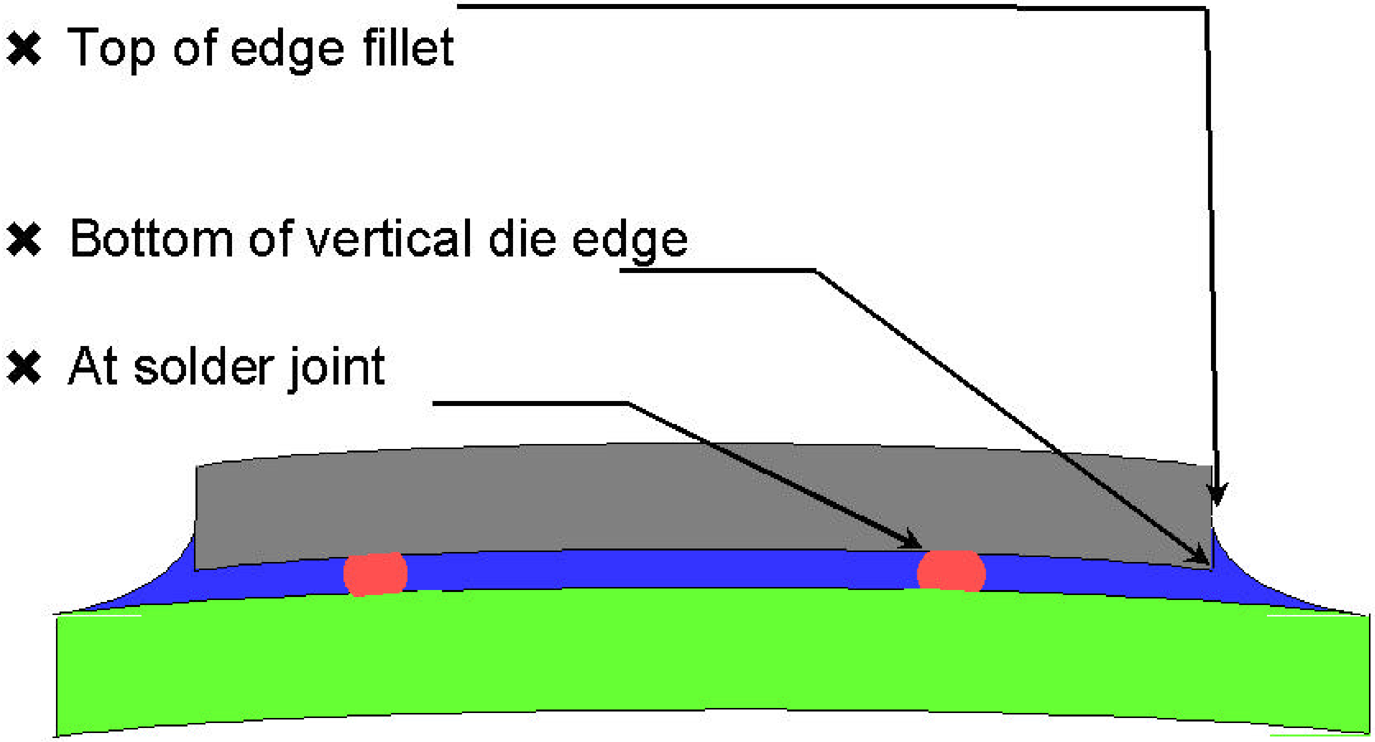
✖ Top of edge fillet
✖ Bottom of vertical die edge
✖ At solder joint

Figure 2.

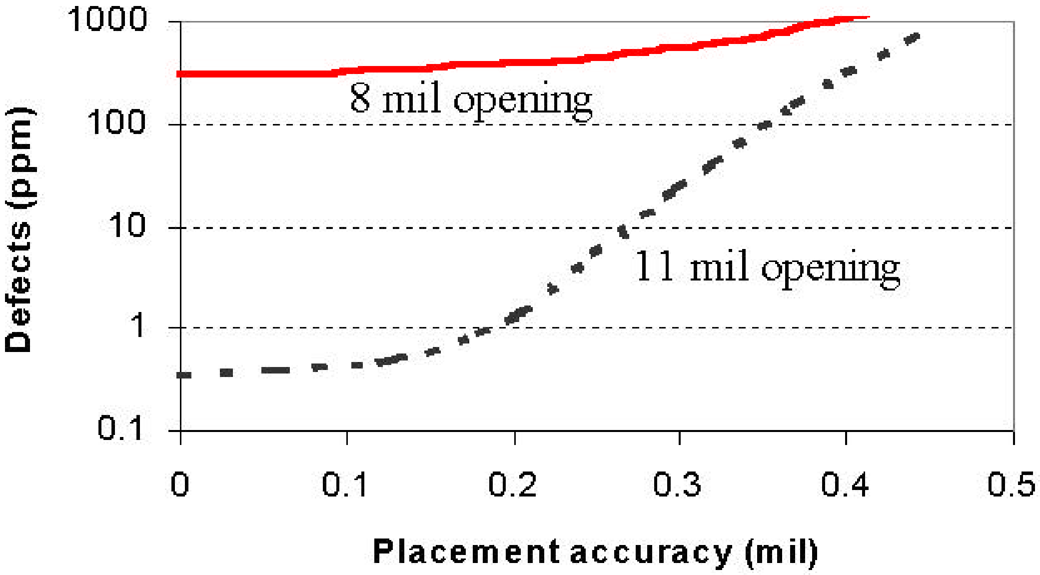
1000
100
10
1
0.1
Defects (ppm)
8 mil opening
11 mil opening
0
0.1
0.2
0.3
0.4
0.5
Placement accuracy (mil)

Figure 3.