

Flip Chip - Integrated In A Standard SMT Process

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This paper reviews the implementation of a flip chip product in a typical SMT production process. Several modifications in equipment, materials and processes were required. Flip Chip is not “just another” package on the board. A number of manufacturing related issues needed to be addressed. Fluxing and Underfill processes were the most obvious areas. Additional attention needed to be paid to yield and quality related issues. This paper reviews these manufacturing issues and discusses how they were solved for a specific product. The process development was performed in partnership with a customer and Universal’s process lab and was based on research results of the Advanced Process Lab.

Introduction

A reduction in cost resulting from higher yields and a reduction in process steps made the conversion of this product family, from wire bond as COC (chip on ceramic) on conductive adhesive to a ridged flex board with flip chip and SMD components in reflow technology, attractive. The product incorporated standard SMT components, mainly 0402 and 0804 and three flip chip components. The flip chips were bumped with eutectic solder. The pitch varies from 350-400 µm. The layout of the dies

required an additional redistribution process that will be eliminated in future products by design for flip chip to further reduce costs.

The board thickness was 0.6 mm. Due to the thin board, all process steps were performed on specially designed carriers, that follow the substrate through all process steps. These carriers simplify the handling while supporting the substrate during printing and protecting it from warpage and deformation due to sagging in the reflow and curing ovens. An integrated clamping mechanism was designed to avoid interference

with the printer. The selected material - IPC Plus from EMC - has a low thermal mass to make uniform heating in reflow, during underfill and curing, easier.

Process Discussion

Figure 1 provides an overview of the process and material-related process parameters as well as the production equipment-related issues. The required changes to a standard SMT process will be discussed for our application in the following section.

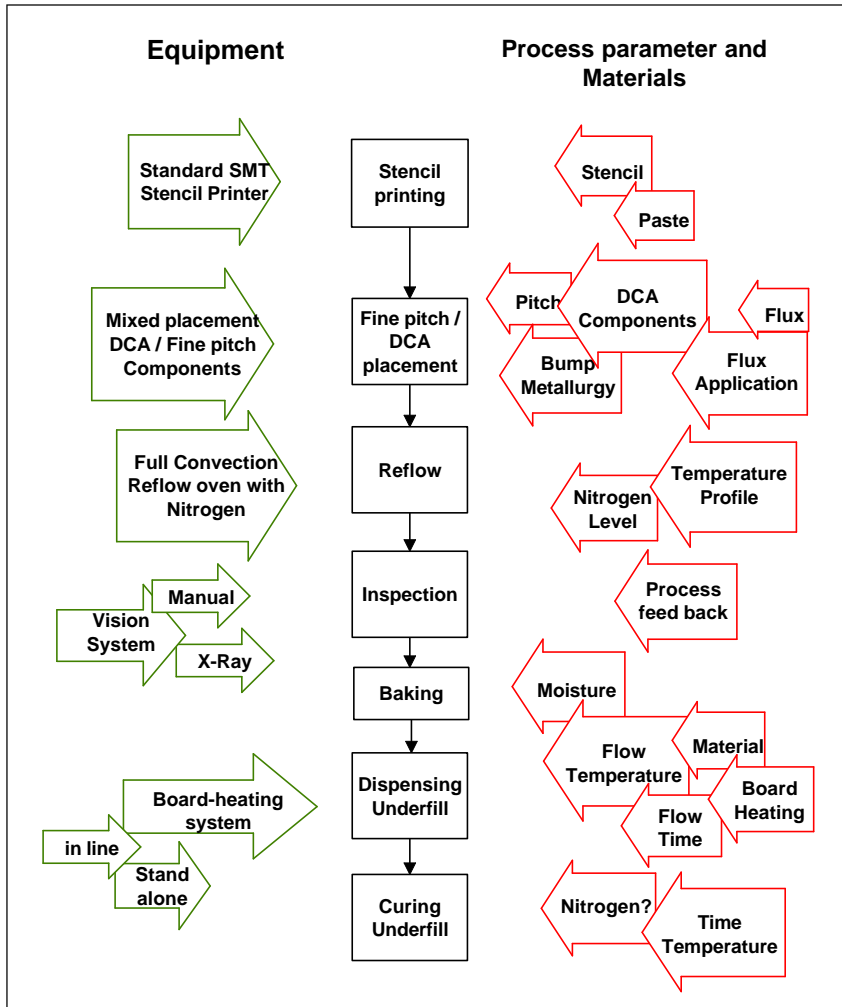


Figure 1 - Process Flow Issues

The process flow shown in Figure 2 reflects the implementation of the additional process steps required for Flip Chip. While the Flip Chip Placement can be integrated in the placement machine together with other SMT devices, the underfill process requires special equipment.

The production line was split into a placement and reflow segment and a separate section with underfill and curing.

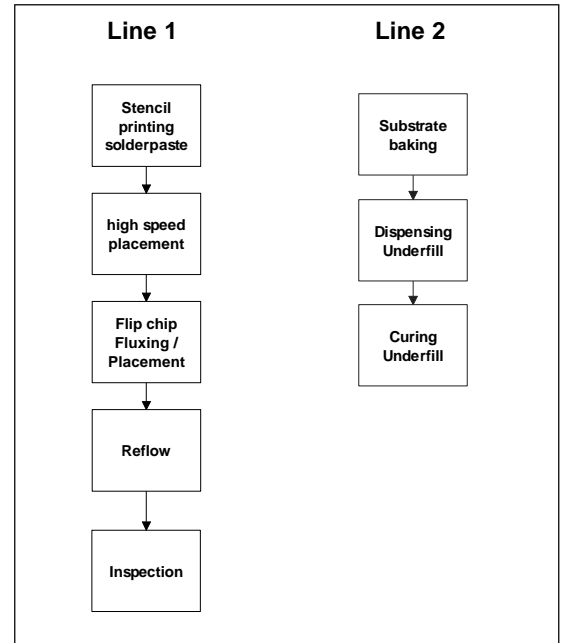


Figure 2 - Process Flow

The flip chip components were handled out of trays. There are several configuration choices that need to be made when considering flip chip assembly on a pick and place machine. They include optical resolution, lighting geometry, processing capability, pick and place tooling, and substrate lifter tooling. Since the interconnect medium of a flip chip is a solder bump, simple die edge techniques are inadequate for locating and placing flip chips. To avoid the possibility of placing flip chips in the wrong orientation, the programming bump pattern used for recognition should be asymmetric. The pick and place machine must have the optical resolution, lighting geometry and the processing capability to locate a pattern of bumps on the bottom side of the flip chip. The pick and place machine must then possess the intrinsic accuracy to place the die precisely on a substrate. In addition, pickup tooling must be properly sized and of the correct material such that when a die is dipped in flux (thin film flux application) it is not dropped in the flux applicator and there is a clean release when it is placed. And finally, the under board support must rigidly capture the substrate so that there is no movement in the substrates due to die placement contact. As

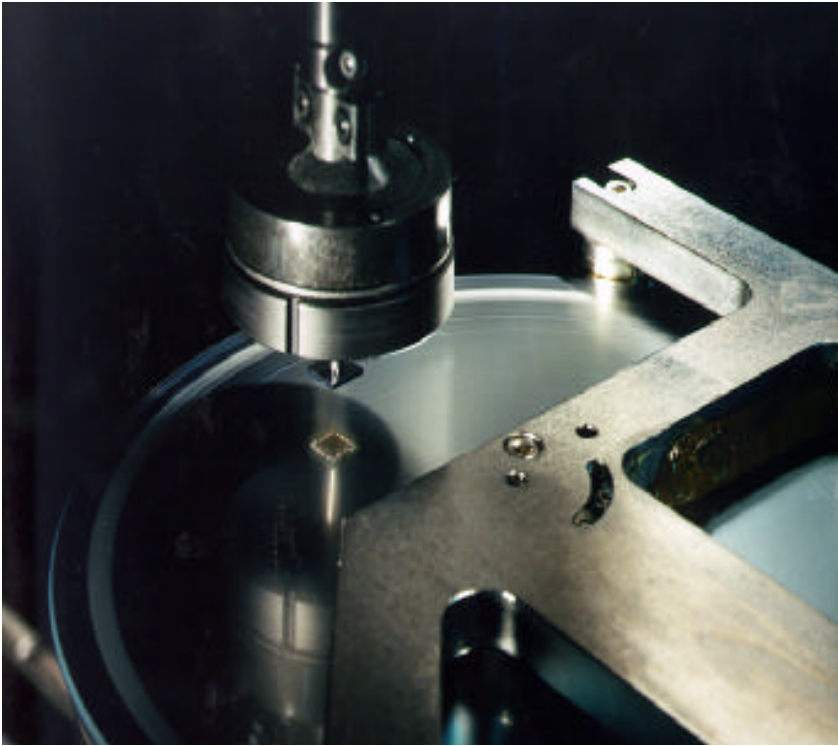


Figure 3 -Dip Fluxing

always, there will be other issues that are specific to a given process that must be considered when choosing a pick and place configuration.

The material and method of flux application have significant impacts on reliability and yield. Dip fluxing and spray fluxing are the most commonly used methods. Most of the fluxes used for spray fluxing are so called “no residue” fluxes with an alcohol content of 98 - 99 %. The fluxes are sprayed on the substrate before placement and the alcohol evaporates rapidly at room temperature. The remaining flux does not provide sufficient tackiness to hold the flip chip in place during board handling and reflow and frequently results in movement of the die.

As a result, a dip-flux process was chosen to apply a tacky flux to the flip chip components. The honey-like no-clean flux is applied in a 75 μm thick film on a rotating plate using a doctor blade (see figure 3). The die bumps are dipped in the flux and placed onto the substrate. Compared to liquid fluxes, which provide no tackiness for the die, tacky paste fluxes will hold the die in place during handling. As a result, problems due to handling are unlikely. The choice of flux and encapsulant is influenced by the die passivation, bump metallurgy, substrate,

solder mask, pad metallurgy and the use environment. A series of benchmark tests using test-die, followed by tests on prototype products were performed to determine the optimal material selections for the product reliability.

The knowledge of bump height distributions and possible bump defects is essential in determining the process window for the dip fluxing. The minimum flux film thickness depends on the bump height variations within a die. To ensure good soldering of the eutectic bumps on the die, all of the bumps have to be dipped in the flux.

To establish a process window for the fluxing, experiments on bare laminate were performed. Flip chips were dipped in flux, placed on a bare copper board with OSP coating and reflowed in various environments. The dies were then sheared off and the wetted solder diameter on the substrate measured. A larger wetting area indicated better wetting performance of the different no-clean fluxes. The flux thickness and reflow oven atmosphere were varied from 12 μm to 35 μm and 200 PPM - 24% Oxygen (air). Figure 4 shows the wetting performance versus atmosphere in the reflow oven. No significant sensitivity to the amount of flux used on the dip fluxer could be seen at any given oxygen level. All the fluxes used showed a need for an inert atmosphere during reflow. The oxygen level needs to be less than 1000 PPM to achieve good soldering results. See Figure 4.

The yield of the placement process is largely dependent on various parameters. In order to study the sensitivity and to find an optimum design, Monte Carlo simulations were performed using the following input parameters:

- Board tolerance (Solder mask, Copper layer)
- Pad design
- Placement accuracy

It is not surprising that the soldermask tolerance is one of the major factors for the assembly yields. Figure 5 shows a design of a board for a perimeter array flip chip with 200 μm pitch. Tolerances given in Table 1 resulted in yields not better than 150 PPM due to the accuracy of the board (Figure 6). To achieve reasonable yields the trench has to be opened to 250 μm to reduce the soldermask effect. This will result in collapse of the die and a smaller gap between

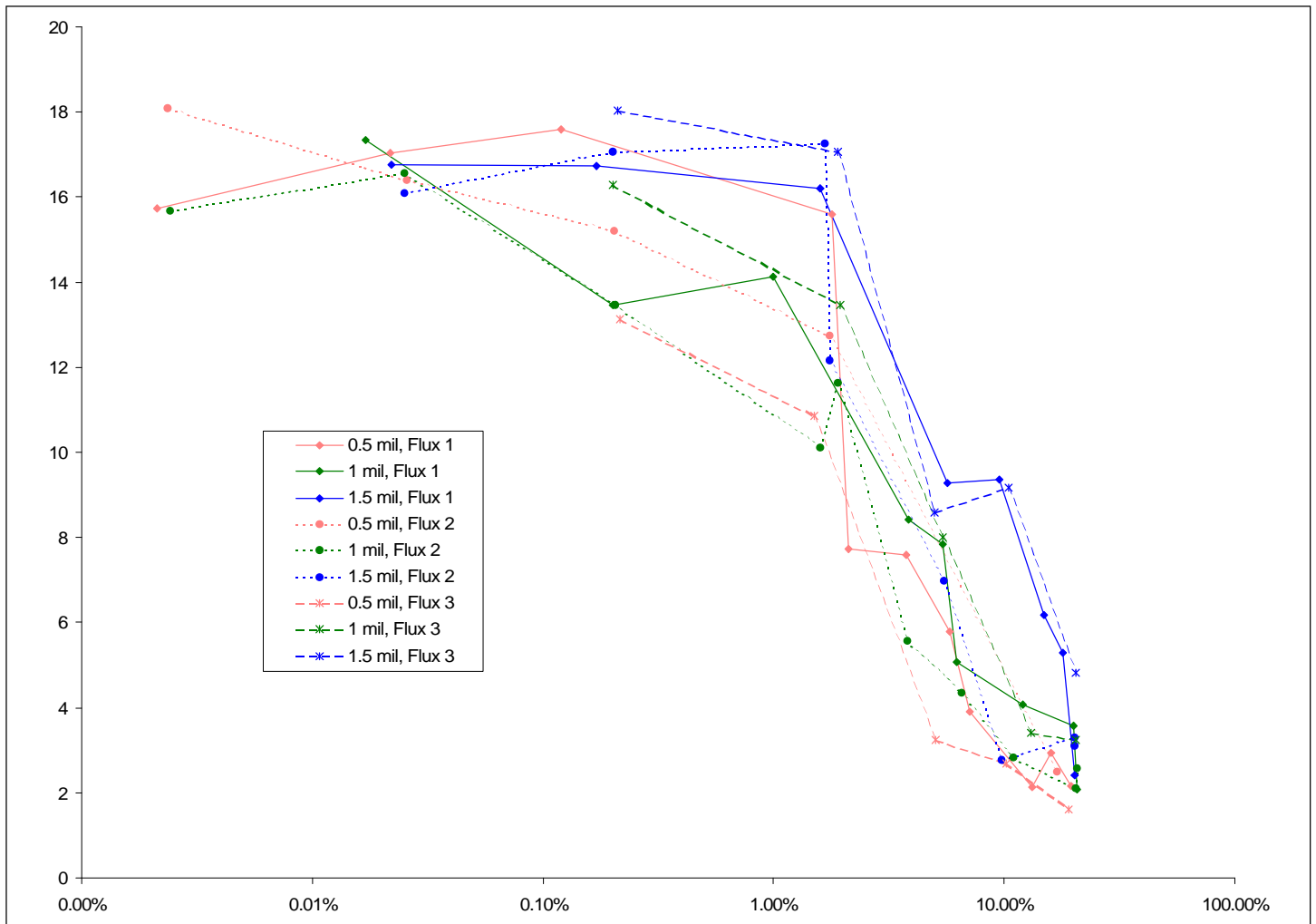


Figure 4 - Process Window for Fluxing

| Table1 - Board Tolerances (All accuracy is given as ± 3 s): | |
|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| Trench width | 200 μm \pm 50 μm |
| Trench position to nominal | \pm 75 μm |
| Pitch | 50 μm pitch, 125 μm lines and spaces \pm 50 μm |
| Line position | \pm 50 μm (obviated by machine using local fiducials) |

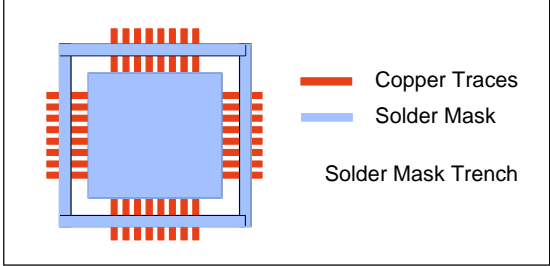


Figure 5 - Pad Design for 200 μm Pitch

die and substrate making underfill more difficult. The limiting factor in this case is clearly the soldermask tolerance.

For the implemented application it was possible, due to the large pitch of 400 μm , to open the soldermask around individual pads and eliminate the influence of soldermask tolerance (see figure 7).

Assuming a tolerance of ± 50 μm for the pad size, the simulation showed the required placement accuracy for this design to be 11 μm (1s) to achieve a PPM rate of 1 or less (Figure 8).

The placement process for this application is therefore relatively non-critical. Smaller pitches (less than 250 μm) would introduce the effect of soldermask registration due to different required pad designs and therefore require drastically better placement accuracy and soldermask tolerances.

The Underfill process is not an established SMT process. Capillary flow fills the 2 - 4 mil gap between the die and the substrate. The

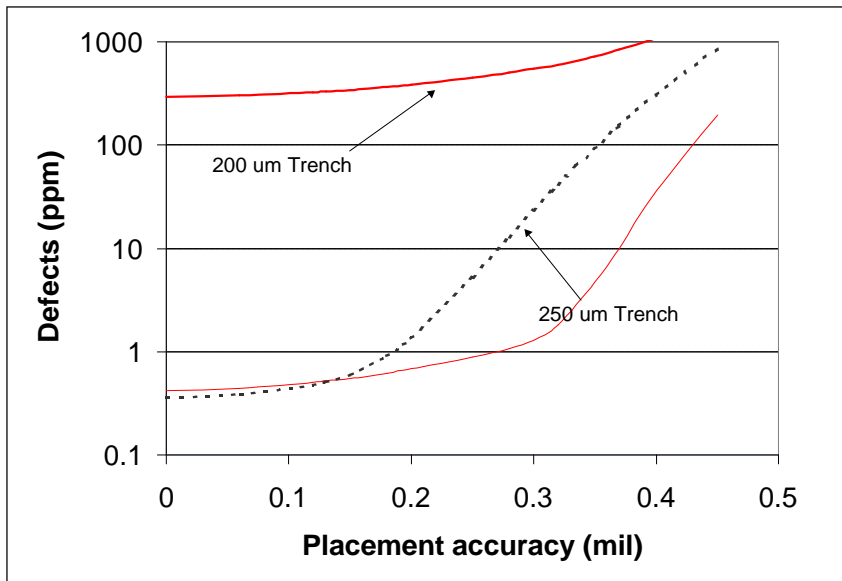


Figure 6 -Yield for Trench Design

material selection becomes one of the most essential parameters for reliability as well as processability.

The fishbone diagram in Figure 9 gives an overview of the parameters having an impact on the underfill process. The multiple interactions between the various different materials involved show clearly that the materials used have to be treated as a system that needs to be reevaluated as soon as one of the materials or the application change. Specifically, the process windows for flow temperatures, dispense pattern and time need to be established for the individual application and materials. Even more importantly, these parameters as well as the choice of materials, will have a tremendous impact on the reliability performance.

The underfill process for the application turned out to be especially challenging because of the space constraints. The available space around the dies did not allow a close-up dispense in all cases. Consequently, dispensing is only possible on one side of the die. An underfill material that forms fillets by itself was therefore required. After finishing the flow under the die, the underfill has to form the fillet necessary for reliability reasons without an additional close-up dispense step. This added an additional criterion for the material selection. Figure 10 shows the chosen dispense pattern.

Contamination of board and die during handling can have a major impact on the underfill process and overall reliability. Because of the

robustness of the soldering process a clean room is not required, although handling boards with gloves and protection of the boards from contamination, dust particles and chemicals is mandatory before underfill curing. Board cleaning after misprints or contamination of the board during repair needs to be avoided. Experiments with moisture exposure of assemblies before underfill showed an impact on the reliability performance. Unfortunately, the tolerable exposure to moisture depends on substrate design and materials as well as the reliability requirements. A two-hour board baking at 125°C before underfill was sufficient for the application to remove any accumulated moisture.

Inspection of materials and testing in the production is necessary to assure high yield in production and acceptable reliability.

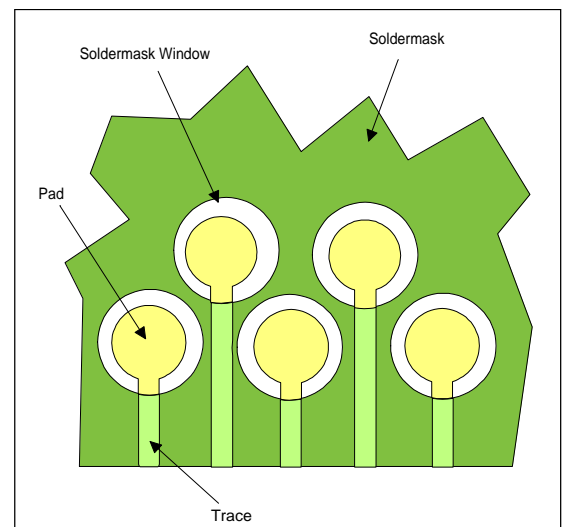


Figure 7 - Soldermask Design for 400 μm Pitch

The assembly yields and necessary process parameters depend, as discussed, on the substrate and die quality. Consequently, the quality of these materials needs to be monitored.

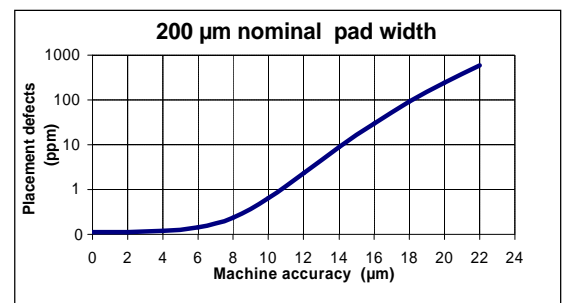


Figure 8 - Yield for 200 μm Nominal Pad Size

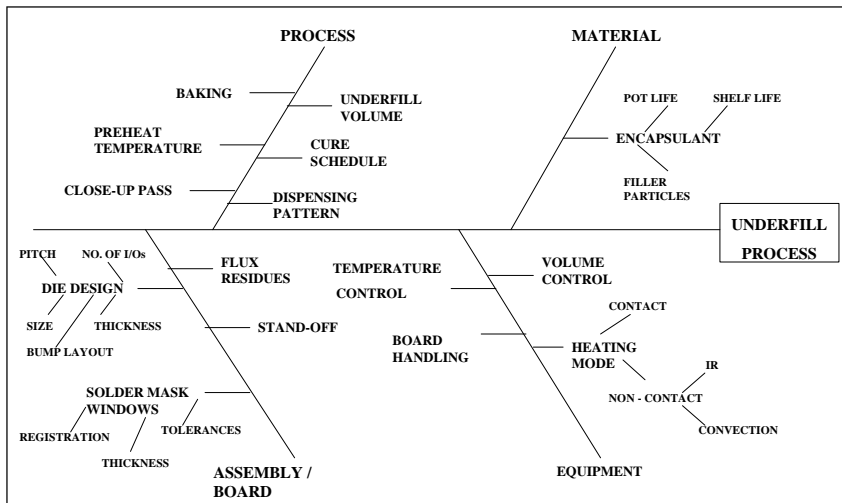


Figure 9 - Factors Influencing the Underfill Process

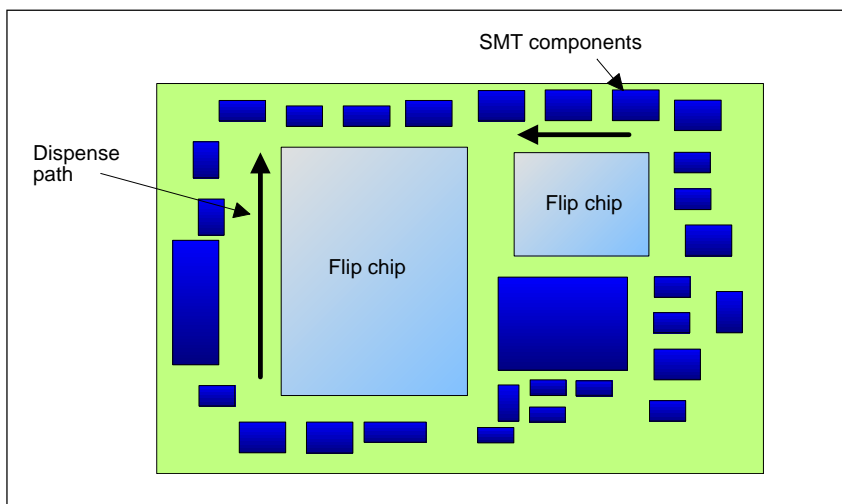


Figure 10 - Dispense Pattern

Specifically, any process changes like new cleaning procedures or process flows, etc. for the substrate, as well as any changes in the bumping technique and underfill material, need to be reported by the supplier to evaluate the impact on the process. Additionally, the substrate tolerance needs to be monitored closely to assure high yields in assembly.

To assure quality it is required to understand the bumping process and monitor the bump height distributions. In addition, shear tests of the bumps can disclose systematic interface weaknesses of the bump. Depending on bumping technology, a change in failure mode or shear force can indicate systematic problems with the wafer lot. A change could indicate a weakness and possible interface problem of the

under bump metalisation (UBM) with the die or solder bump.

Lot to lot changes of the encapsulants' properties are often difficult to detect. Underfill needs storage temperatures below - 40°C and rapidly ages at room temperature. Temperature variations that occur during shipping or storage can substantially alter the performance of the underfill materials. Simple standardized tests can be performed to monitor changes in the encapsulant batches. Possible tests are a flow test and a test measuring the wetting angle to the substrate.

The flow test can be performed between glass slides and used as a benchmark to determine qualitative changes in the flow performance of the material. The wetting angle of the underfill to the substrate and die can be measured using samples that are partially underfilled and then cross-sectioned. Change of the wetting angle can indicate surface contamination of substrate or die passivation as well as changes in the underfill material itself.

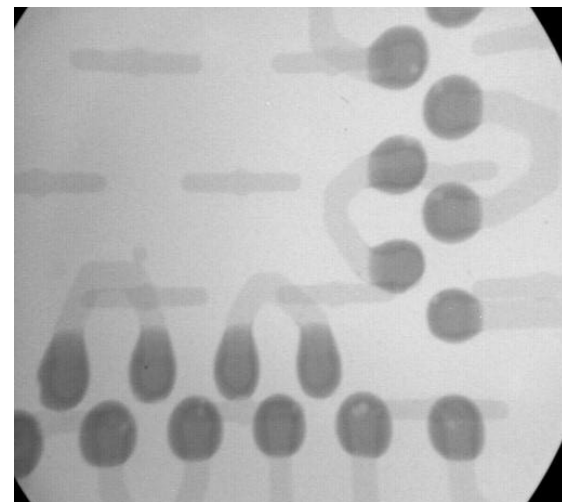


Figure 11 - X ray of Solder Joint

Offline X-ray test equipment is being used to do regular testing of the soldering quality. Because of the circular pad design with attached traces, a two-dimensional x-ray is, in this case, sufficient to determine the solder joint quality. Figure 11 shows the visible joint formation due to the pad geometry. Non-wetted pads on the substrate are easy to detect, because the bumps will not deform during reflow.

Other observable failures are solder voids and solder bridging. Solder bridging can be caused

by solder extrusions filling the voids touching the soldered bumps. Depending on the bump pitch, these voids can link two solder joints and cause bridging during thermo-cycling or additional reflow. *Figure 12 and 13* show some typical failures. Due to the wide pitch of 400 μm the risk of failures like these is very small for this particular application.

The underfill quality of the process was monitored with acoustic microscopy. Since the submersion of all assemblies in water for testing is not desirable, spot checks were performed in order to detect voids and incomplete flow. Alternatively, a destructive test can be performed by grinding the die off the assembly in order to inspect the underfill layer.

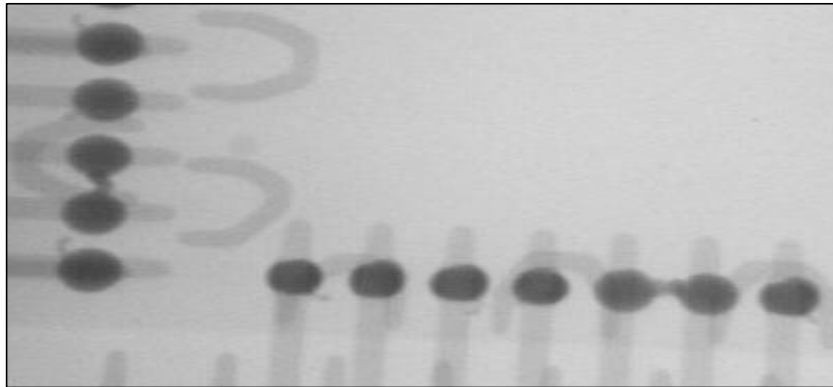


Figure 12 - Bridging Caused by Solder Extrusions

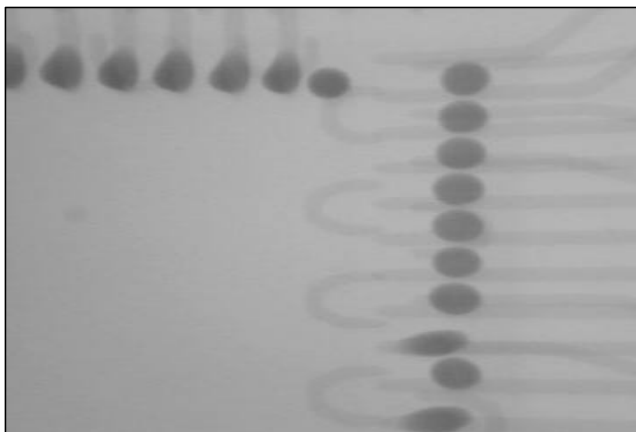


Figure 13 - Non Wetted Pads

Conclusion

The discussed example shows that various issues need to be addressed for the integration of flip chip into a standard SMT process flow. The material selection of flux and encapsulant is influenced by the die passivation, bump metallurgy, substrate, solder mask and pad metallurgy. Process windows and robustness make a dip fluxing process preferable. Board design and component pitches will significantly impact the assembly yield. For the underfill process, the process windows for flow temperatures, dispense pattern and time need to be established for the individual application and materials. Monitoring of the incoming materials like bump height distribution and underfill flow performance as well as board quality is important because of the number of interactions in the process, specifically the underfill process. Contamination of board and die during handling can have a major impact on the underfill process and overall reliability. Additional board baking might be required to assure sufficient reliability and good underfill performance.

New materials and processes make it very difficult to maintain high yields, acceptable quality and a “competitive edge”. Ongoing support and partnership with a large, application-relevant R&D organization is required. Nevertheless, standard solutions for conservative applications in terms of pitch and reliability requirements are becoming possible.

The selection of the material system is the key to required reliability as well as assembly yield. Different from other technologies it is possible to implement flip chip assembly in a step-by-step fashion as far as investments in facilities, equipment and training are concerned. The decision to go with flip chip in a specific application may then be made on a case-by-case basis.