Flip Chip Research at UIC

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Abstract

The present document offers a brief overview of ongoing research into flip chip related packaging issues within the SMT Laboratory at Universal Instruments Corporation. In spite of 8 years of in-depth research our work still seems far from done. The major part of the research is funded by the Area Array Consortium which was established specifically to fund research into design, materials, and process related microelectronics and optoelectronics packaging issues.

Introduction

Over the past 8 years we have researched and resolved a very broad range of flip chip related issues including effects of chip layout, UBM, wafer bumping, backlapping, dicing, substrate technologies, flux selection and fluxing, placement, reflow, bake-outs, underfilling, underfill materials, curing, heat spreader or lid attach, component balling, contamination, handling, and inspection. These issues were carefully considered from the perspectives of materials compatibilities, assembly yields and quality, reliability, and cost. While by no means independent of each other each issue has formed the basis for one or more Master's thesis or Ph.D. dissertations, and we by now feel that we have established a considerable fundamental understanding, as well as a series of practical tools and guidelines. Nevertheless, as is so often the case more knowledge has also helped formulate more complex questions. The following text offers a brief outline of our ongoing research in this area.

Research

Over the years our work has included both rather large chips (up to 27mm) and quite fine pitches (down to 4mil), and further work is forthcoming on both. Currently, however, a substantial part of our work is being conducted on moderate sized 8 mil pitch, single perimeter array chips and, to a lesser extent, on 5mm and 10mm full area array die with a 10 mil pitch within and between rows. Needless to say much of our work continues to revolve around reliability issues, as outlined below, but substantial effort is also invested into questions of design, assembly yield and defect prediction, materials and process alternatives and optimization. While considerable work still remains to be done on eutectic Sn-Pb attachment to FR-4 or BT type substrates we are currently conducting a major study on all aspects of no-Pb soldering. In addition, we are investigating issues involved in soldering to Au-bumped die, flip chip attachment to flex and ceramic substrates, and reflow in air as opposed to a nitrogen ambient.

Flip Chip Reliability

More than anything else reliability concerns and the resulting need to underfill have significant impacts on almost all aspects of flip chip assembly. Notably, process windows are largely limited by assembly defect and reliability issues. Unfortunately the most attractive designs and materials combinations, from a process and/or cost perspective, often do not offer the best reliability. Even for modest reliability applications process optimization often requires a simultaneous optimization of the reliability within the given constraints.

Previous research has provided us with an in-depth understanding of individual, competing, damage mechanisms contributing to failure under various combinations of processing, storage and service conditions. It has become clear that mechanisms which often dominate life in service are not properly addressed within current accelerated test protocols. Ongoing work has revealed separate contributions of aging, even in an inert environment, and exposure to humidity. Either of these effects depend on design, process and materials combinations in different fashions and, to further complicate matters, the individual dependencies are often not simple. Current tests do not accelerate these mechanisms sufficiently and indications are that they may be quite seriously misleading in terms of relative ranking of materials, etc.

It is also important to realize that almost all accelerated testing relies on an explicit or implicit interpretation in terms of ‘life in service’. First of all, it is vital that relative comparisons between alternative materials, designs, and/or processes reveal ‘the best one’ as far as service life expectancy is concerned. Furthermore, while absolute accuracies may be extremely limited we still need to extrapolate test results to decide what is sufficient to ensure a reasonable ‘life in service’. If necessary, even extremely conservative estimates (lower limits) of life would be likely to have tremendous consequences. So far, however, noone has been able to do this with any degree of credibility.

We are therefore conducting fundamental studies of individual damage mechanisms through combinations of modeling and specifically designed experiments. The aim is to be able to distinguish, and separately accelerate, dependencies on humidity, temperature and aging. We already believe to be able to extrapolate appropriate sets of accelerated tests to service conditions, but this will require extensive validation.

The same and complementary studies are also continuing to address changes in damage mechanisms during accelerated testing. There is good hope that we will be able to account for ramp rate (thermal shock) effects in cycling, but the validity of highly accelerated tests such as pressure cooker or HAST is being critically assessed.

Somewhat independently of actual life assessment we do, of course, also still need for our assemblies to perform well in ‘standard’ tests such as thermal cycling/shock and, for components at least, the JEDEC Level 3 popcorn test. Because of the looming transition to no-Pb soldering with the correspondingly higher reflow temperatures in subsequent board level attach emphasis is on peak temperatures of 260^{o}C in the latter.

Ongoing work is exposing ‘all’ combinations of 30-40 encapsulants and 20-40 tacky or liquid no-clean fluxes to liquid-to-liquid thermal shock, air-to-air thermal cycling, and high temperature JEDEC Level 3 testing. This obviously includes monitoring of the progression of solder extrusions, encapsulant fillet cracking and delamination where possible, as well as detailed failure analysis, in order to distinguish between individual damage mechanisms. Importantly, great care has been taken to ensure that the matrix covers realistic manufacturing process variations.

Yield/Defect Prediction & Design for Assembly

Tools are being developed to help in trade-off decisions as well as design, materials selection and process optimization. Actual flip chip assembly yields obviously depend on a very large number of factors as well as on the definition of a ‘defect’. Notably, the level of statistics involved makes an experimental (empirical) assessment of relevant defect levels at best impractical until the manufacturing stage.

We have taken a step-by-step approach to this. So far, we have developed and validated computer programs addressing the defect mechanisms that are most sensitive to chip and substrate pad design, placement and collapse in reflow. We continue to make these programs more user friendly and realistic. Notably, flip chip assembly yields are quite sensitive to the detailed solder joint shapes associated with various contact pad configurations. We are currently incorporating the results of extensive numerical simulations of such shapes into the appropriate yield program.

Another potential source of defects is fluxing. Depending on the choice of flux and fluxing method shorter, possibly damaged, solder bumps may not always reach sufficiently deep into the flux in time to ensure robust soldering. It is anticipated that our studies on the fluxing alternatives (see below) will provide the necessary understanding and input for us to model this as well.

Flip Chip Assembly in Air

There is an overwhelming interest in avoiding cleaning under the flip chips, i.e. using no-clean fluxes or reflow encapsulants (see below). Because of flow behavior and influence on reliability only a rather small subset of the former are actually acceptable for flip chip applications. In general, no-clean fluxes tend to have relatively low activity and usually require nitrogen reflow to ensure good wetting and collapse of the solder joints to their equilibrium shapes. Good wetting promotes high soldering yields and sufficient bonding to (intermetallic formation with) the contact pads to survive thermal cycling. Depending on the specific substrate pad design a full collapse may be necessary to compensate for the combined effects of substrate warpage and ball height and pad size variations. Also, an incomplete collapse is likely to be less reproducible and thus leads to larger variations in gap size (standoff) between chip and substrate. This would lead to increased edge fillet height/thickness variations in an automated underfill process and thus significantly affect process development and assembly reliability.

It would, however, be attractive to eliminate or reduce the need for a nitrogen reflow ambient. Nitrogen tends to be expensive, particularly if the oxygen level has to be less than a few hundred ppm. Also, current recommendations for eutectic Sn/Pb based 0201 assembly specifically involves air reflow. Integration with these would thus also require flip chip reflow in air.

It is, in fact, not difficult to identify no-clean tacky fluxes which allow flip chip assembly in air reflow. However, wetting and collapse is often strongly reduced and the quality of the joints, as reflected in the resulting thermal cycling resistance of the underfilled assemblies, lower.

We have identified a couple of tacky fluxes that offer complete wetting and collapse of Sn/Pb flip chip joints in air with a properly optimized profile, as well as several that seem to work well with 1000 ppm O_2. Work is ongoing to identify liquid fluxes for use with the DispenseJet (see below) for soldering in air. Alternative pad finishes (immersion Ag or Sn) are being investigated as well. In all cases the consequences for assembly reliability is being quantified. Chemical compatibility issues are expected to favor different underfill materials with the new fluxes, and resistance to JEDEC Level 3 testing, aging and moisture is likely to be affected.

Attempts will also be made to address no-Pb soldering in air, although there currently seems to be little hope for this except perhaps with a reflow encapsulant (see below).

Fluxing Alternatives

Both liquid and tacky fluxes may be applied inside the placement machine. However, we have not found significant advantages to the dispense of a liquid flux in the machine. In general, liquid fluxes are distributed across the substrate (die site), not just located on the bumps or contact pads where they are needed. Reliability and, in particular, moisture resistance of the underfilled assembly is therefore usually reduced. Liquid fluxes also offer relatively little tack. In contrast, no-clean tacky fluxes which are reasonably compatible with preferred underfill materials, and thus offer better reliability, have been identified. However, dipping the solder balls into a thin film of a tacky flux inside the placement machine may slow down flip chip placement by up to 10-15%. It is therefore often attractive to apply the flux outside the placement machine.

The use of a reflow encapsulant dispensed onto the substrate before it enters the placement machine is dealt with separately below. We have also made stencil printing of both tacky fluxes and reflow encapsulants work very well, but this is only really attractive for component manufacturing.

We are therefore conducting an in-depth study of the DispenseJet system from Asymtek, which offers the potential for dispensing a much thinner, uniform layer of a liquid flux in selected regions. We have identified the requirements on a flux for it to be considered optimized for the jet, and we are currently working on specific processes that minimize the flux (residue) level without unnecessarily endangering assembly yields. Special attention is being paid to the effects of solder bump damage on fluxing and joint formation (see above). As optimized processes are established, the resulting reliability of flip chip assemblies underfilled with various encapsulants is then quantified. It is anticipated, for reasons of both chemical and mechanical compatibility, that different encapsulants may be preferred than with current tacky fluxes.

Reflow Encapsulants

An increasing number of materials have been developed that can be dispensed before chip placement, serving as fluxes during reflow and subsequently turning into an underfill layer. Potential benefits include the elimination of requirements for nitrogen reflow and the removal of the fluxing process from the placement machine (see above). The latter has also been achieved with the DispenseJet but not yet with an optimized process and established reliability.

A reflow encapsulant for Sn-Ag-Cu solder would be extremely attractive and several new products are under investigation. Current liquid or tacky fluxes do not even allow defect free soldering of this in high-purity nitrogen (see below).

We have investigated a large number of materials for Sn/Pb soldering in terms of process windows and reliability. By now we have established an in-depth mechanistic understanding of the individual issues and process steps, and written a detailed ‘process cook-book’. Not surprisingly, the approach proves quite sensitive to substrate dryness, but bake out requirements were found to vary strongly with material and substrate. Benchmark numbers for currently best achievable thermal cycling/shock resistance have been established.

We continue to test new materials for both Sn/Pb and Sn-Ag-Cu solder, the former in more or less detail depending on robustness of the soldering process and on thermal cycling resistance, taking the effects of unavoidable fillet thickness variations in high volume manufacturing into account. Process windows will be further quantified for the best ones in terms of substrate bake-out requirements, acceptable storage between bake out and dispense, and dispensability. Sensitivities to aging, moisture, and high temperature JEDEC Level 3 testing are addressed.

Underfill Dispense Process

Based on 7+ years of experience we have developed an in-depth 'manual' outlining practical issues and suggestions for selecting dispense equipment and underfill materials, practicing with both, developing the actual process for any given product, and finally failure analysis (trouble shooting). Particular emphasis is placed on the establishment of a systematic database to allow for rapid, product specific process development and trouble shooting later on. This document is updated considerably every year. The goal is to develop a true step-by-step 'cook book' that can be used to train new underfill process engineers, as well as supporting experienced people. Based on user feedback it is being thoroughly restructured this year.

In general, materials continue to be characterized in terms of dispensability and flow, automatic fillet formation and wetting, as well as reliability and compatibility with fluxes, solder masks, chip passivations, pad and solder metallurgies. Current work emphasizes the risk of voiding allowing for solder extrusions and bridging at moderate and fine pitches. This can be affected by the solder mask technology and design, as well as by underfill and flux selection, but also by the dispense process and, notably, the details of the cure process. Efforts are ongoing to establish general guidelines for how to minimize or, when possible, eliminate voiding.

Transfer Molding

A concern in flip chip component (BGA, CSP) manufacturing is the performance of underfilled and subsequently overmolded parts with the new, higher reflow peak temperatures and JEDEC Level 3 testing (260^{o}C, see above). Problems observed appear to be affected by the chemical compatibility of flux, underfill, mold compound, etc. We are currently addressing this, as well as thermal cycling performance. It has also been suggested that optimized overmolding may improve the thermal cycling resistance of components assembled using reflow encapsulants, but again life may be more complicated than that. We plan to address this as well.

A potentially attractive alternative concept is to simultaneously underfill and overmold the component, thus eliminating the need for a separate underfill step and significantly increasing throughput. Several groups are currently working on the development of transfer mold processes and appropriate materials for this purpose. So far, however, the simultaneous void free underfilling of 50-100 assemblies, as required in production, has usually been achieved on substrates with holes under the die. This is not attractive for general use. It appears that vacuum assisted molding may eliminate the large void under the middle of the die, but materials modifications seem to help as well.

Working with a number of partners we have been testing a number of materials in JEDEC Level 3 (260^{o}C) and cycling. Initial results suggest good reliability, including at least as good a thermal cycling resistance as achieved with the best capillary underfills.

No-Pb FC Assembly

The use of no-Pb solder has unique consequences for flip chip applications. Because of the small dimensions involved reduced wetting and solder joint collapse may easily affect assembly yields. Together with a narrower reflow process window it may also lead to a broader gap size (standoff) distribution and thus problems for an automated underfill process. The choices of contact pad metallurgy and reflow profile, as well as repeated reflows, have been seen to seriously affect both intermetallic formation and 'bulk' solder composition after reflow. This has significant consequences for the solder joint fatigue resistance. Finally, the solder alloy may affect underfill delamination in cycling quite strongly.

So far a very large range of reflow profiles and fluxes, including several developed specifically for the purpose, all failed to ensure consistently defect free flip chip assemblies. Conducted with a pad design offering particularly robust assembly none of our experiments revealed electrical opens or reliability problems, but wetting was inconsistent and self centering was poor. We are continuing work to resolve this with new profiles, fluxes, and pad finishes. Notably, a large number of dedicated liquid no-clean fluxes are being tested using the DispenseJet. After process optimization promising materials are tested in terms of the effects of the residues on underfilling and final reliability (resistance to cycling, humidity and aging). It is anticipated that different underfills will be 'preferred' than for Sn/Pb solder.

Although certain similarities exist, the detailed metallurgical effects (intermetallic formation, precipitation, composition changes, grain growth) are very different from, and generally much more complex than, what we are used to from Sn/Pb. Notably, even minor differences in reflow profile or aging conditions may severely affect materials properties, as did extra reflows before or after underfilling. Our in-depth studies on such metallurgy issues are continuing.

Previously we have considered Sn/Ag/Cu/In, Sn/Ag/Bi, and Sn/Sb as well as Sn/Ag/Cu which seems to be a current industry favorite. However, we have also initiated studies of Sn/Cu and Sn/Ag bumped chips as evaporation or plating of a ternary alloy tends to pose problems.

Ultra-Fine Pitch

Solder bumped chips tend to be limited at fine pitches when compared to modern wire binding. An alternative involving Au stud bumped die and preapplied solder on the substrate is therefore being proposed, but questions of intermetallic formation raise obvious concerns. We are currently conducting a detailed investigation of this approach.

Flip Chip on Ceramics.

Over the years we have gathered considerable experience with regards to flip chip assembly onto conventional ceramic substrates. Most recently we conducted a limited effort on issues that affect assembly, i.e. the statistics of pad sizes and locations. Unlike for organic substrates random variations of these parameters within a given substrate were found to be significant, and the placement yield prediction software was updated to address this in a user friendly fashion.

Indications are that both flux residues and moisture may affect underfill voiding quite differently than on typical organic substrates. We therefore expect both JEDEC Level 3 performance and the effects of aging and moisture exposure of the final product to be different as well. This would have consequences for materials selection and process, notably bake out requirements.

We are currently planning a new study of flip chip on LTCC ceramic substrates, addressing both assembly and reliability issues.

Flip Chip on Flex

Rigid flex applications do not always pose unique problems, but dynamic flex certainly do. Not surprisingly, fixturing for assembly has proven to be an issue, and our experiences have led to some design recommendations. Also, dynamic flex substrates usually involve a so-called coverlay, rather than a rigid soldermask. Large coverlay registration tolerances and adhesive bleed tend to limit design options, often requiring a single large mask opening or very wide trenches along the edges. This has been seen to affect the underfill process as well as the gap under the chip after solder joint collapse. Some practitioners limit solder spread and collapse by reflowing in air with a flux intended for nitrogen use only, but that does not seem attractive. Notably, it has been seen to reduce the solder joint fatigue resistance in spite of the greater standoff. Also, any approach that prevents collapse to equilibrium shape will cause greater chip-to-chip variations in that standoff. The statistics of this may have consequences for an automated underfill process and, together with bump height variations, potentially for the assembly yields. Luckily, we were able to establish a process that ensured a 1.5-2mil gap without this.

Substrates with a regular photoimageable solder mask in the die region show promise, but the effect of single sided mask application on flex warp has to be addressed. Previous results show that balancing is an option but far from trivial. Cost would have to be assessed both for this approach and for nickel plating with selective gold coating in the intended pad area only.

Reliability issues include possible new effects of underfill properties now that this layer may provide the more critical mismatch. The sensitivity to moisture and aging, and the compatibility of underfill, flux, substrate material, solder and pad metallurgy, are expected to be unique to dynamic flex. Depending on the application the question obviously remains to which extent thermal cycling resistance is still a concern at all, or whether vibration and handling is.

We are currently quantifying the performance of specific flip chip assemblies on flex substrates in thermal shock and cycling. Our plans for further studies will depend strongly on getting access to the relevant technologies.

Summary

In spite of a wealth of understanding and knowledge gathered over the past 8 years a number of issues are found to warrant continued research. The capillary underfill dispense process still remains more of an art form than a technique. Tools offering quantitative predictions of assembly defect levels associated with specific design, component, equipment, and process parameters are proving invaluable in, for example, substrate design but substantial refinements and additions are possible. Reflow in air offers substantial savings and is clearly feasible, but it has been seen to reduce reliability and an incomplete solder joint collapse would have to be carefully accounted for in some designs. Recent progress shows promise of resolving this. Removal of the fluxing process from the placement machine would enhance throughput significantly, but current reflow encapsulants cannot compete with the reliability of regular underfills and no-clean fluxes. Both the DispenseJet approach and underfilling by transfer molding do seem quite promising, however. The introduction of no-Pb solders obviously introduces a whole new range of issues and concerns, including the sensitivity of solder properties to small (unavoidable) variations in process parameters or assembly parameters. Even if the small flip chip solder volumes are somehow exempted from the switch to no-Pb solder, components will still have to survive JEDEC testing with high peak temperatures. Finally, it is becoming increasingly obvious that important flip chip damage and degradation mechanisms are not properly addressed by common accelerated tests. Needless to say, an understanding of reliability which would allow even an extremely conservative estimate of ‘life in service’ would be likely to affect future implementation and application of flip chip technology tremendously. Ongoing research is addressing this as well.